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Low noise front end ICECAL ASIC for the upgrade of the LHCb calorimeter

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ABSTRACT: A fully differential ASIC with cooled input termination is presented as a solution for the Upgrade of the Calorimeter front end electronics. The LHCb experiment needs to increase about ten times the integrated luminosity in order to study new physics. The increase in signal has to be compensated reducing the gain of the photomultipliers which implies stringent noise requirements. The proposed solution offers an active termination at the input and avoids the noise originated by the use of a resistor. The circuit is based on a two interleaved channel with a first amplifier stage, a switched integrator, and a Track-and-Hold. Two prototypes have been implemented and tested in SiGe BiCMOS 0.35um technology.

KEYWORDS: Calorimeters; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons)

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1 The LHCb upgrade

The LHCb [1] is one of four large experiments of the Large Hadron Collider (LHC) based at the CERN laboratory near Geneva. It is expected to collect an integrated luminosity which will largely cover its proposed physics program. However, in order to distinguish among models of new physics, a large increase in data rate is needed. LHCb collaboration intends to upgrade [2] the detector during the planned long LHC shutdown in 2016.

1.1 LHCb calorimeters upgrade

We consider here the RD work for the upgrade of the front end electronics of the calorimeter subdetectors. The analogue signal processing in the present ECAL Front End (FE) board is mostly performed by a shaper ASIC that integrates the photomultiplier (PMT) pulse, which has been clipped at the PMT base for pile-up rejection. Indeed, to ensure a satisfactory independence of successive sampling, the residue of a signal 25ns after the sampling time is required to be less than 1% [3]. The PMT signal is transmitted from the detector through a 12m 50Ω coaxial cable to the FE board located in the crates at the calorimeter platform.

1.2 Motivation

A new front end board is required due to changes of gain and low noise of the analog electronics and to the need of the new data transmission method (using the GBT [3]) at 40MHz.

The PMT gain has to be decreased by a factor 5 in order to tolerate the increase in luminosity, and avoid ageing problems. Otherwise PMT would die rapidly. Therefore, the preamplifier gain has

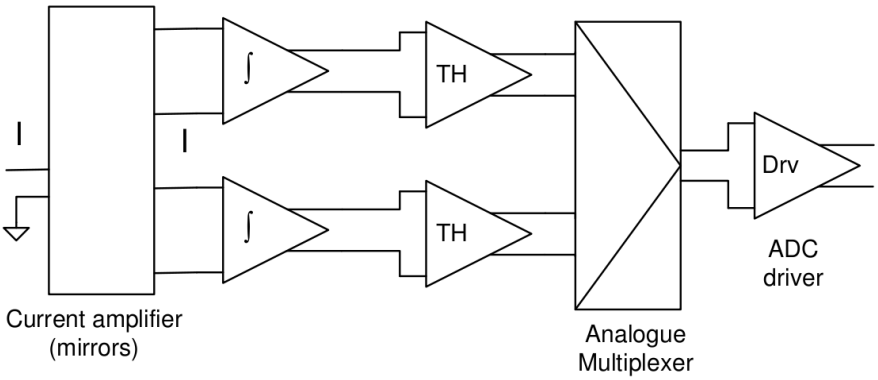

Figure 1. Channel design scheme.

to be increased accordingly and, at the same time, decreasing the input noise; the total input referred noise voltage of the front should be smaller than 1 LSB. An ASIC development was proposed because the FE board has 32 channels and a transistor level approach was required for any active termination scheme. For a 12 bit data range, the total input referred noise is limited to 1nV/$\sqrt{}$Hz for moderate source impedance. Consequently, a 50Ω termination resistor is not acceptable.

There is an alternative solution using discrete elements [5]. It would be possible to remove the clipping at the PM base (at the detector level) and increase the signal at the amplifier input as two thirds of the signal is lost by clipping. Then, the clipping would be performed after the amplification in the Front End.

2 Channel design

The presented implementation of the ASIC includes two alternated switched signal paths where the input current is first amplified and converted to differential signaling in order to be integrated through a fully differential amplifier with capacitive feedback. Since no dead time is allowed and high quality delay lines cannot be easily integrated, the solution is to alternate every 25 ns between two integrators and to reset one integrator when the other one is active. A fully differential signal processing is adopted in order to minimize the impact of common mode noise, which is important in a switched system.

The different stages of the channel are represented in figure 1. The input stage is a current preamplifier with a cooled termination for reduced noise. Afterwards, the signal is integrated with switched integrators. A track-and-hold samples the integrated signal and is sent to the analogue multiplexer that selects the correct subchannel. And, at the end, an ADC driver is planned to be used to match the ADC input impedance.

The channel operation is depicted in figure 2 from simulations. The input pulse signal (from a measured PMT clipped pulse) is first integrated in subchannel 1 during the first half of the clock cycle. At the same time, the output charge from the integrator is transferred in the hold capacitors of the T/H while the other subchannel integrator is in reset state.

During the next half clock cycle, the integrator of subchannel 1 is being reset and subchannel 2 performs the integration of the tail of the signal. At the same time, the output of the T/H is

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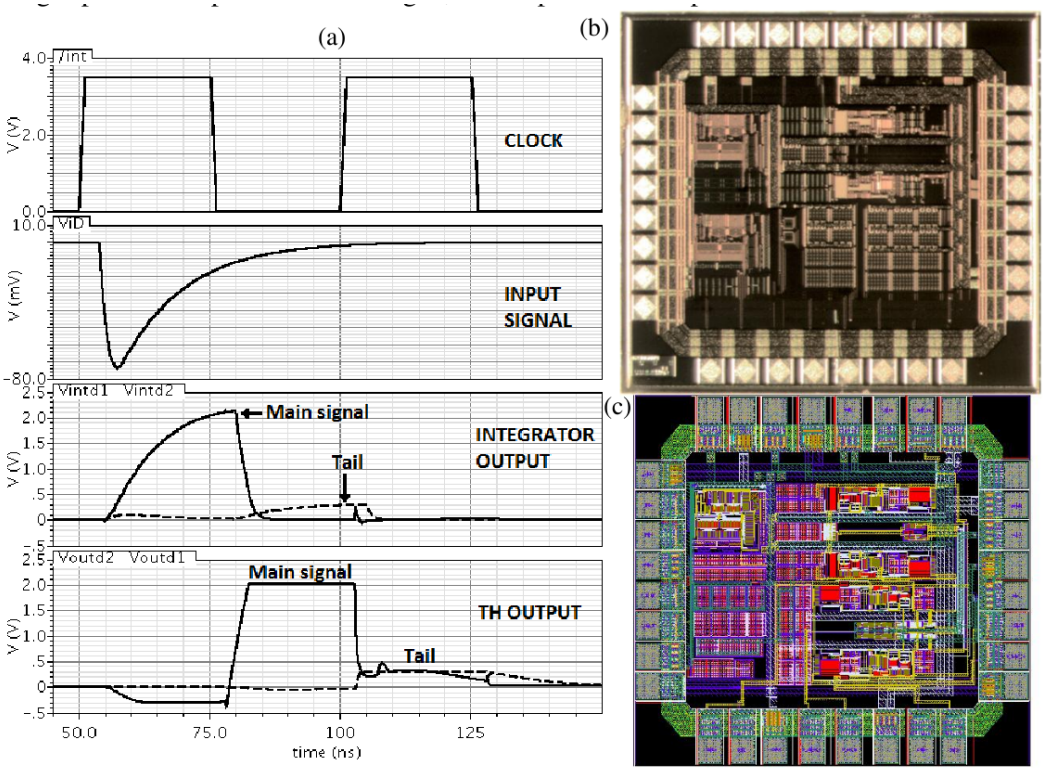

Figure 2. (a) Channel operation simulation (left). The main signals are represented for both subchannels (clock, input, integrated signal, and T/H output signal). (b) Photograph (right top) of the ICECAL1 prototype. (c) Layout (bottom right) of the ICECAL2 prototype.

swiftly stabilized with the main signal output in subchannel 1 and in the next half clock cycle the tail integrated signal has already been tracked and it is hold at the output of subchannel 2.

Due to the high gain bandwidth, DC open loop gain, and slew rate of the FDOA, the overall power consumption is notable in simulations: about 35mA in total. Further studies of the packages power dissipation are envisaged, but no problem is expected.

2.1 Current preamplifier

The Input amplifier is made of a "super common base" input stage with double feedback and it presents an electronically cooled termination. The two current feedback loops (figure 3) are used to decrease and control the input impedance of a common base transistor with emitter degeneration and provide additional transconductance linearization. The input impedance can be derived as:

$$Z_i \approx \frac{1/g_{m1} + R_e}{1+K} + \frac{K}{1+K} m R_f \tag{2.1}$$

The current mode implementation has several advantages with respect to previous designs [6, 7]: low voltage, DC coupling (no external components or additional pads), all nodes have low impedance (less prone to pick up noise), and ESD robustness is improved (no MOS transistor gate or bipolar base is connected to the input pad).

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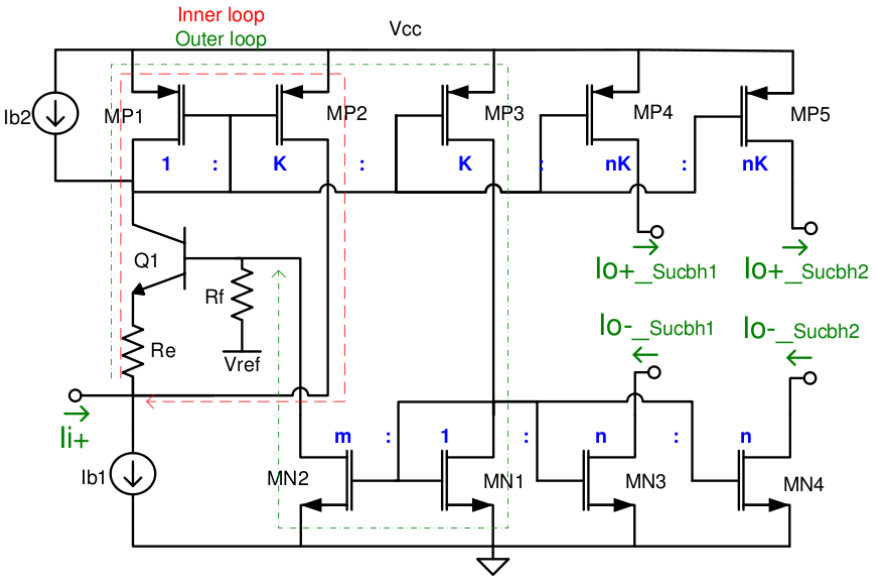

Figure 3. Current preamplifier input stage scheme.

Table 1. Integrator stage specifications.

Integrator Specification	*Value*
Integrator peak plateau	4ns
Linearity	$< 1\%$
Residue	$< 1\%$ after 25ns
Reset time	10ns

2.2 Switched integrator

The switched integrator is based in a fully differential operational amplifier (described in 2.4), feedback capacitors, discharge resistors, and CMOS switches to perform the operation. figure 4 shows the scheme of the integrator and table 1 indicates the main specifications of the stage. The feedback switches are on during the integration cycle. When the integration finishes, the reset cycle starts; two switches connect the inputs to ground and the feedback ones are off. In order to obtain a fast reset and avoid residual amplification, fast discharge switches are utilized. The integrator capacitors are discharged in less than 10ns.

Two extra feedback resistors are added with 100ns time constant in order to improve the integration peak plateau to minimize possible problems originated by clock jitter. They also help cancelling the slow component remnant of the clipped signal.

2.3 Track-and-Hold

A Track-and-Hold for a 12 bit ADC is added after the switched integrator. It is based on flip around architecture with bottom plate sampling (figure 4), which help in reducing the tracking capacitor charge error and accomplish better linearity. The feedback design is preferred respect an open loop one for improved linearity and accuracy.

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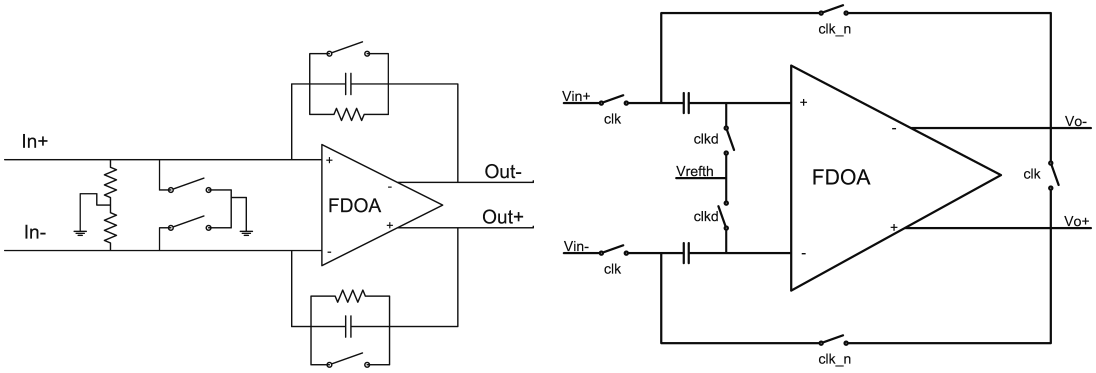

Figure 4. Switched integrator and Track-and-Hold schemes.

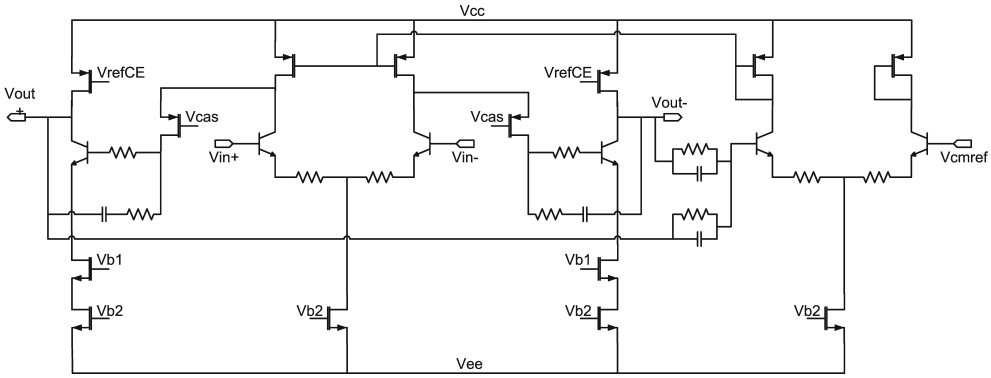

Figure 5. FDOA schematic.

The amplifier specifications were defined from the accuracy required with 12 bit and by using half of the clock for slewing and settling the output signal. The DC gain needed for an accuracy of half a bit, for 12 bit data range, assuming linear settling is $A_0 > 2^{13}/\beta$. Selecting the lowest β of the configurations of the T/H, A_0 must be greater than 80 dB.

In order to allocate all the slewing in the first 1/8 clock period, the amplifier slew rate must be greater than 0.6 V/ns. The rest of the half period (3/4 of a clock cycle) is left for settling, which leads to a gain bandwidth product of 190MHz.

The fully differential amplifier presented in 2.4 it fulfills most of the T/H specifications except the DC gain (A_0), but this only affects linearly and it can be calibrated afterwards.

2.4 Fully differential operational amplifier

In order to achieve the specifications of the circuit, the FDOA must comply with the characteristics exposed in table 2 for moderate capacitive loads (below 15 pF). Another important characteristic for the accuracy of both the integrator and the T/H stages is the gain bandwidth product. This leads to a relatively high power consumption of about 9 mA.

The FDOA (figure 5) consists in a bipolar pair input with emitter degeneration, a folded cascode stage, a second Miller stage with a bipolar output in common-emitter amplifier configuration, and a common mode feedback circuit.

Table 2. FDOA specifications.

FDOA Parameter	*Value*
Gain bandwidth	500 MHz
DC gain	$>$ 70 dB
Phase margin	$>$ 65^o
Slew rate	$>$ 0.4 V/ns

2.5 Choice of technology

Taking into account the design, a SiGe BiCMOS technology is preferred. There are two main reasons for this decision. First, SiGe heterojunction bipolar transistors (HBTs) have higher g_m/I_{bias} than MOS transistors which allows obtaining less noisy designs and lower input impedance variation. And, second, SiGe HBTs display higher transition frequency ($f_T > 50$GHz), easing the high gain bandwidth product (GBW) amplifiers design.

AMS BiCMOS 0.35μm is the technology selected. It offers an HBT transition frequency high enough, and deeper submicron CMOS technology is not needed nor wanted in the proposed design. With four channels per chip the transistor integration density is not an issue. Deeper submicron would imply the use of smaller voltage power supply and worse matching.

AMS technology radiation hardness will be studied. At the moment, some preliminary measurements seem to indicate that this technology is robust enough for the present project.

3 First prototype: the ICECAL1 chip

A first prototype (called ICECAL) of input stage of the chip including preamplifier and switched integrators was designed in Austriamicrosystems 0.35μm SiGe BiCMOS technology, with 3.3V power supply.

The purpose of the ICECAL1 was to test the key points of the novel circuit idea: the input impedance controlled by current feedback, its low noise performance, and the linearity through the dynamic range. Otherwise, it was also required to check the critical aspects related to a switched solution: offset between channels, switch related noise, and the plateau of the integrator output (which takes into account the effect of the clock jitter versus the signal).

3.1 Measurements

The input impedance control by current feedback is properly working as is shown by measurements of the input signal reflections.

The input and output signals of the prototype are shown in figure 6 as captured in the test set-up. The source signal corresponds to the waveform generator that provides the pulse. Then, after 12m cable, the signal at the chip input is included. It can be observed also the two subchannels outputs and the 40MHz clock.

The termination at the input of the chip can be tested from the first reflection of the signal seen at the output of the waveform generator after 50ns after the pulse has reached the input of the ASIC prototype. There is a 1–2% of systematic deviation due to process variations and parasitic

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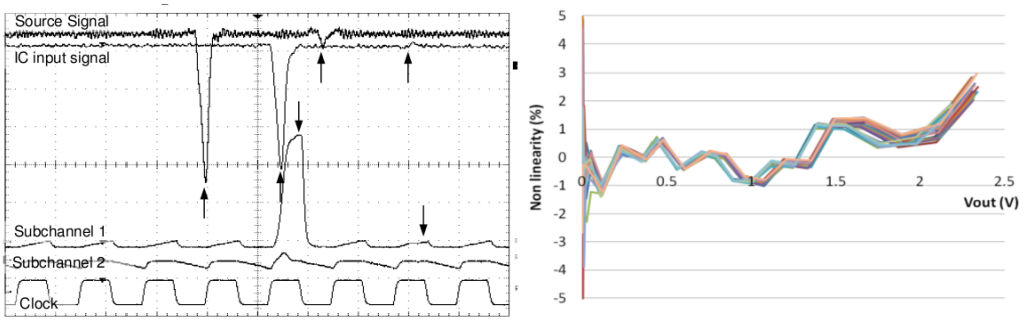

Figure 6. Input and output signals of an ICECAL1 oscilloscope capture (left) showing the signal reflections, and the relative non-linearity for the 12 first prototypes (right).

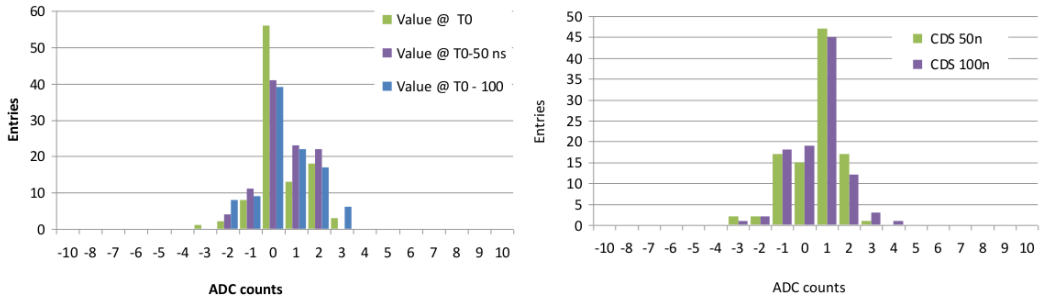

Figure 7. Pedestal measurements histogram (left) and after dynamic pedestal subtraction (right).

resistances that can be corrected. Otherwise, the variation of the reflection coefficient as a function of the integrated input charge of the pulse shows less than 0.5% variation, which implies that the 0T stage feedback based design operates linearly in the whole dynamic range.

The noise can be extracted from histogram studies of the pedestal value evaluating the standard deviation from a Gaussian fit. figure 7 represents the pedestal for three consecutive cycles showing a noise of 1.8 LSB rms. If correlated double sampling, or dynamic pedestal subtraction, is applied, the noise is reduced to 1.25 LSB rms, close to the value 1 LSB rms from the simulations. This indicates, presumably, that there is a low frequency pick up noise due to the chip test socket.

The offset at the output is generated by the integration of the offset current at the preamplifier stage. The interesting value is the difference between subchannels as long as there is an AC coupling between the ASIC and the ADC. Then the offset is confined to values below 5% of the full scale range (2V).

Relative non-linearity is defined as the normalized deviation from a linear regression (not relative to the full scale). As can be observed in figure 6, except for very low amplitude values for which the error is high, the non-linearity is below $\pm 1\%$ for the full dynamic range.

4 Conclusions

An integrated circuit for the LHCb Calorimeter electronics upgrade has been presented which is reported to be able to cope with the upgrade stringent noise requirements. Its architecture is based

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on a current mode preamplifier with cooled termination for reduced noise, and two fully differential interleaved subchannels which include a switched integrator and a Track-and-Hold.

Measurements of the first prototype show that the design complies with the basic requirements for the LHCb Calorimeter Upgrade. The input impedance controlled by current feedback is stable for the full scale range and shows low noise performance. Linearity is enough for the full dynamic range.

The switched solution critical aspects have also been tested. The offset between channels is limited to less than 5% of the scale range and the impact of the residual amplification is measured below 2% of the main signal. Although the plateau of the integrator output does not last long enough, a feedback resistor in parallel with the integrator capacitor is expected to fix it.

Next steps consist in adding the possibility to adjust some of the parameters of the circuit. The parameters include the input impedance, to be able to compensate for process variations, the gain to adapt for different PMT gains, and the integrator feedback resistor to compensate for different pulse shapes. Another upgrade will be to add a DC offset at the current preamplifier output in order to exploit the full dynamic range of a differential circuit, which is two times larger.

Acknowledgments

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