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A Really Low Voltage Solar MPPT

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ACTA DE L'EXAMEN
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Reunit el Tribunal qualificador en el dia de la data, l'alumne

D. Pau Coma Ramirez

va exposar el seu Treball Final de Màster, el qual va tractar sobre el tema següent:

A Really Low Voltage Solar MPPT

Acabada l'exposició i contestades per part de l'alumne les objeccions formulades pels Srs. membres del tribunal, aquest valorà l'esmentat Treball amb la qualificació de

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Abstract

Energy harvesting or scavenging describes the process of extracting useful electrical energy from other ambient energy sources. Three main sources of ambient energy include vibrational, thermal and solar energy. Through the use of special materials that have the ability to convert one form of energy into the other energy harvesting can be accomplished. Even though most of the energy coupling materials currently available have been around for several decades, their use for the specific purpose of energy harvesting has not been thoroughly examined until recently, when the power requirements of many electronic devices has reduced drastically.

Of the three main sources of energy, the solar cell has been the most effective is achieving this translation of energy. Solar cells have been widely used in low power electronics such as calculators where several of these are placed in series to achieve a voltage high enough to operate the device. Further serialization and scaling of solar cells allows solar arrays in terrestrial applications to reach enough voltage to generate three phase voltages for energy distribution in the main power grid. The scope of this project deals with the output characteristics of one solar cell as the energy source. The voltages range from 600mV to 3V depending on the solar radiation levels and the technology of the cell itself. The desired output voltage is 12V. Several circuit topologies to achieve this high voltage gain are presented and discussed. Algorithms to track the maximum power output of the solar cell are presented. As a result a practical circuit design is proposed to allow for further future research on the problem to be solved.

Summary

As the need for remote operation and desired portability of electronic devices continues to increase, power for these devices becomes more of a concern. Remote applications are powered mostly by batteries that are either recharged or substituted on a regular basis. The more remote the location is, the bigger the challenge becomes of replacing this energy source. The substitution of this energy source by that of the solar energy eliminates the need to revisit the applications location. This thesis focuses its research around a solar cell as an energy source to recharge some batteries to allow for night time operation. The design requirements derive from the SalleSat scenario. SalleSat is a cube that the university plans on putting in orbit. The power source will be four solar panels where each solar panel is planned on being tracked individually. The objective of the thesis is to introduce and introduce several voltage boosting topologies considered for this application. The equations defining the behaviour of each topology will be presented and in the case of the classical boost topology, the process of deriving them is also presented. A design will be proposed and the adequate, existing component values will be calculated noting the implications of each choice. The design is to track the maximum power point of the solar cells and thereby a microcontroller is included, not only to implement the algorithm but to be able to give feedback to the other elements in the cube. Several tracking algorithms are presented and compared. The result of this thesis is a broader insight to the solution to the energy scavenging problem in the given scenario and a proposed design who's design process helps in gaining insight to other posible problems.

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Introduction

The problem posed which directed the research for this project it its direction comes from a bigger project called SalleSat. SalleSat is a nano-satellite that the university plans on launching in a Low Earth Orbit, adhering to the popular CubeSat kits. Compared to traditional multi-million-dollar satellite missions, CubeSat projects have the potential to educate the participants and implement successful and useful missions in science and industry at much lower costs. These cubes are normally powered by 4 solar panels. This thesis focuses its discussions on one solar panel. Given the dimensions of the cube, 10x10x10cm, the solar panels are actually a single solar cell. The terms panel and cell when referring to the solar cell will be used interchangeably.

A solar cell voltage ranges from 0.7 V to 2 Volts depending on the technology of the cell, the ambient temperature and the solar radiation it is exposed to. The electronics which are going to be in the cube consist of a CPU, powered at 3.3V, a radio transceiver, powered at 12V, and a couple other boards powered at voltages at or in between the two specified. So the problem has been posed.

Objectives

The objective of this thesis is to research methods how to extract the power of the solar cell efficiently and convert the cell voltage to required voltages of other boards within the SalleSat. A study of the proposed ideas and walk through of a proposed real life design to achieve the desired function should broaden the readers perspective in how to best achieve an efficient conversion.

Thesis outline

The thesis is organized into six chapters.

Boost Topologies Here three different boost topologies are presented and discussed: Standard Boost, Multi phase Boost and Tapped inductor Boost.

Deriving Classical Boost Equations An explanation and demonstration of how the equations for the standard boost come to be.

Design Specifications According to our space scenario and data from CubeSat we define the specifications for the application to implement.

Component Calculations Components of the standard boost to achieve the design specifications are calculated and selected from available market components.

Maximum Power Point Trackers An introduction a brief explanation on the inner workings of several MPPT Algorithms

Proposed Design With the calculated components and a micro controller a board is designed as a proposed solution prototype to evaluate.

Chapter 1

Boost Topologies

1.1 Classical Boost

The most basic boosting topology is the boost converter (also known as step-up converter), depicted in figure 1.1.

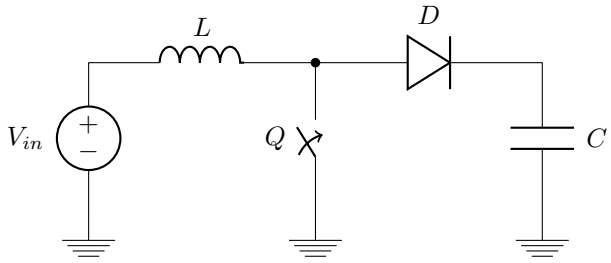


Figure 1.1: Basic boost topology

It is a power converter with an output DC voltage greater than its input DC voltage. L is used as an energy accumulator, C as an output filter, Q and D are the semi conducting switches involved in the conversion.

1.1.1 Operating principle

The key principle that drives the boost converter is the tendency of an inductor to resist changes in current. When being charged it acts as a load and absorbs energy, when being discharged, it acts as an energy source. The voltage it produces during the discharge phase is related to the rate of change of current, and not to the original charging voltage, thus allowing different input and output voltages.

The essential control mechanism of the circuit in figure 1.1 is turning the switching semiconductor switch, Q, on and off. This defines 2 distinct states:

- The ON-state: When the switch is ON, the current through the inductor, L, increases and the energy stored in the inductor builds up.
- The OFF-state: When the switch is off, current through the inductor continues to flow via the diode, D, to the output capacitor, C, and the rest of the circuit connected to the output.

As the voltage builds up the circuit goes through two stages, the transient stage and the steady state stage. The circuit then remains in the steady state maintaining a constant output voltage.

In this steady state, the responses in the circuit are periodic. It means especially that the inductor current is periodic. Its value at the start and end of a switching cycle is the same. The net increase in inductor current over a cycle is zero. If it is non-zero, it would mean that the average inductor current should either

be gradually increasing or decreasing and then the inductor current is in a transient state to later become stable once again in the steady state.

To maintain the steady state, the switch, Q, is responsible for closing the loop. It is assumed that the transition between OFF-state and ON-state become periodic at a fixed frequency we will call f, corresponding to a repetition period of duration T. The time dedicated to being ON versus that of being OFF is defined by the term Duty cycle, d. The switch is ON for a duration of $d \cdot T$ and is OFF for the remaining time in the cycle, $(1 - d) \cdot T$.

As stated before, the current in the inductor at the start of each cycle is the same as at the end of the last cycle. This leaves us with two scenarios, one where the current in the inductor descends to zero before the start of the next cycle, discontinuous conduction mode, and the other where there is a remaining, base, current in the inductor, continuous conduction mode.

1.1.2 Continuous conduction mode

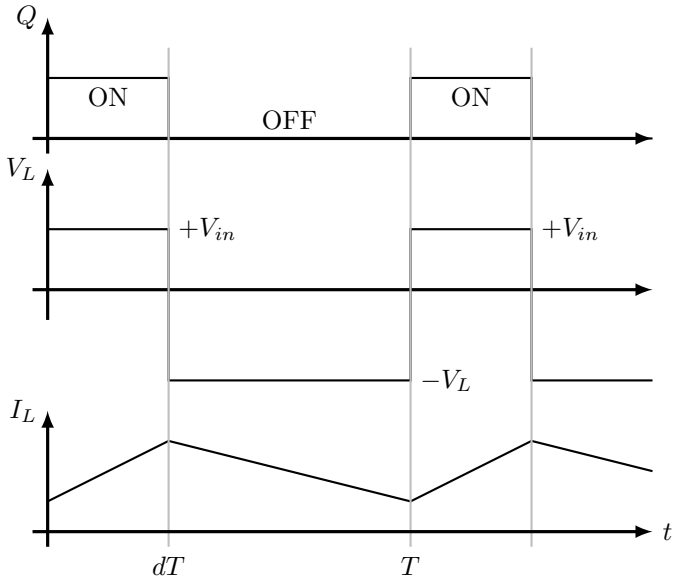


Figure 1.2: Timing of CCM in Boost converter

When a boost converter operates in continuous mode, the current through the inductor, I_L, never falls to zero. Figure 1.2 shows the typical waveforms of currents and voltages in the inductor operating in this mode. The output voltage can be calculated as follows, in the case of an ideal converter operating in steady conditions:

During the On-state, the switch Q is closed, which makes the input voltage (V_{in}) appear across the inductor, which causes a change in current (I_L) flowing through the inductor during a time period (dT) by the formula:

$$\frac{\Delta I_{L_{on}}}{\Delta t_1} = \frac{V_{in}}{L} \tag{1.1}$$

During the Off-state, the switch Q is open, so the inductor current flows through to the output. If we consider zero voltage drop in the diode, D, and a capacitor, C, large enough for its voltage to remain constant, the evolution of I_L is:

$$\frac{\Delta I_{L_{off}}}{\Delta t_2} = \frac{V_{in} - V_{out}}{L} \tag{1.2}$$

In steady state we mentioned before that the net inductor current is zero, $\Delta I_{L_{off}} = \Delta I_{L_{on}}$. Thereby taking the different Δt's, related as $\Delta t_1 = dT$ and $\Delta t_2 = (1-d)T$, into consideration we can formulate a relationship

between the input and output voltages:

$$d \cdot T \cdot \frac{V_{in}}{L} + (1-d) \cdot T \frac{V_{in} - V_{out}}{L} = 0 \tag{1.3}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-d} \tag{1.4}$$

From equation 1.4 it can be seen that the output voltage is always higher than the input voltage (as the duty cycle, d, goes from 0 to 1), and that it increases with d, theoretically to infinity as d approaches 1.

1.1.3 Discontinuous conduction mode

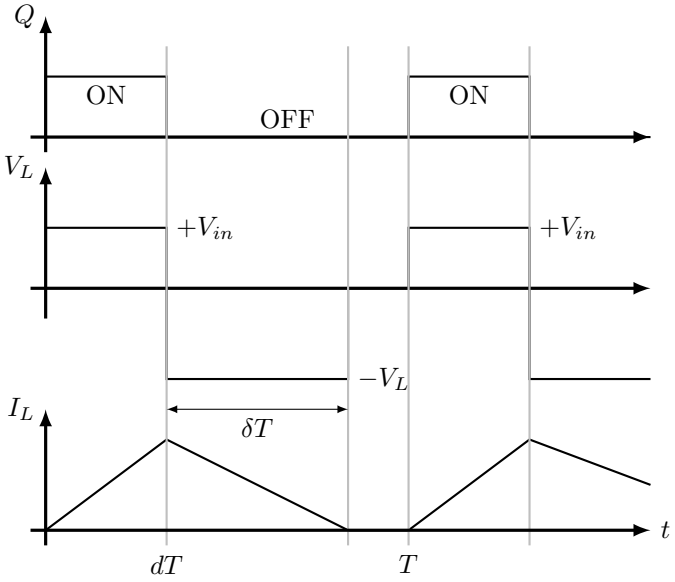


Figure 1.3: Timing of DCM in Boost converter

In some cases, the amount of energy required by the load is small enough to be transferred in a time smaller than the whole commutation period. In this case, the current through the inductor falls to zero during part of the period. The only difference in the principle described in section 1.1.2 is that the inductor is completely discharged at the end of the commutation cycle. This difference has a strong effect on the output voltage equation.

The rate of charge during the ON-state is the same as in CCM, described in equation 1.1. As the inductor is discharged at the beginning of each cycle, the change in current defines the absolute current acquired by the inductor, we will name this quantity I_{peak}.

$$I_{peak} = V_{in} \frac{dT}{L} \tag{1.5}$$

During the OFF-state, the current in the inductor, I_L, falls from I_{peak} to zero in a time δT.

$$I_{peak} + \frac{V_{in} - V_{out}}{L} \delta T = 0 \tag{1.6}$$

$$\delta = \frac{V_{in} \cdot d}{V_{out} - V_{in}} \tag{1.7}$$

As the rate at which the current decreases in the off time is related to the load connected to the converter we will relate the fractional time, δ, to the output current, I_{out}.

$$I_{out} = \frac{I_{peak}}{2} \delta \tag{1.8}$$

Relating equations 1.5, 1.6, 1.7 and 1.8 the output voltage gain can be written as:

$$\frac{V_{out}}{V_{in}} = 1 + V_{in}\frac{d^2 \cdot T}{2 \cdot L \cdot I_{out}} \tag{1.9}$$

In discontinuous operation, the output voltage gain not only depends on the duty cycle, d, but also on the inductor value, L, the input voltage, V_{in}, the switching frequency, $f = \frac{1}{T}$, and the output current, I_{out}.

1.1.4 High gain problems

CCM Gain

For continuous conduction mode, from equation 1.4 it would seem that one could choose an inductance value at random and be able to boost the value to any desired voltage. This is not true, as the boundary is marked by the external circuit consumption. As long as,

$$I_{out} \geq \frac{I_{peak}}{2} \tag{1.10}$$

, then the current the circuit is providing is greater than the change of current acquired during the first phase of the cycle, therefore there must be a remaining current in the inductor, hence continuous conduction mode.

Having defined the values of the components to stay in continuous conduction mode we can choose a voltage gain defined by the equation 1.4.

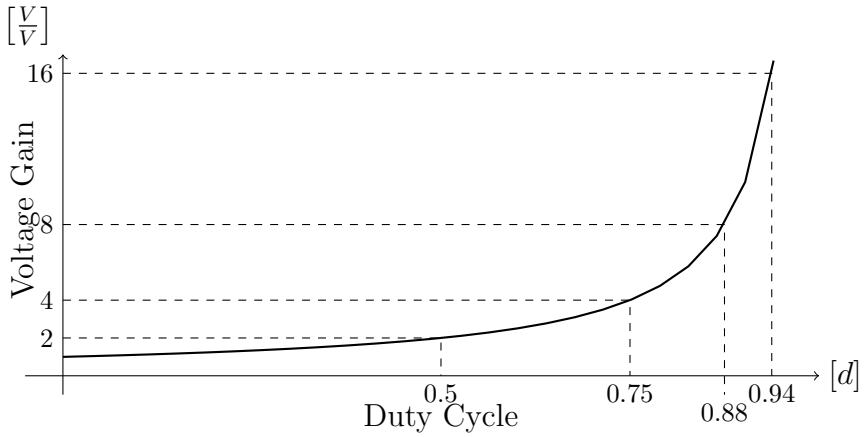


Figure 1.4: Voltage Gain in CCM versus duty cycle

Loop Stability

Inherent to a low voltage boost application comes high gain as we may want to boost the voltage from 1 or 2 volts to 5 or 10 volts. In the case of wanting a voltage gain of 10 we find our selves in the duty range between 0.88 and 0.94, where for a voltage gain of 10 specifically we would want a duty cycle of 0.9 (90%).

The sensitivity of the voltage gain increases exponentially with the gain itself. Depending on the resolution of our switching element we will be able to maintain a stable output voltage or not. Considering a typical switching frequency of 100kHz, to be able to maintain the output voltage of 10V with a permissible ripple of ±100mV our duty cycle can not go beyond 90.1% or below 89.9%. This translates to a resolution of 10 nano seconds. Parasitic elements and temperature variations could well deteriorate our resolution beyond this.

DCM Gain

To simplify the analysis in the discontinuous mode we will define the switching frequency, f, to be 100kHz, the inductance, L, to be 680nF, the input voltage, V, to be 1V and the output current, I_{out}, to be 0.3A.

Given these parameters we need the peak current, $I_{peak} = V_{in}\frac{dT}{L}$ to be greater than 0.6A. $0.0408 \leq d$.

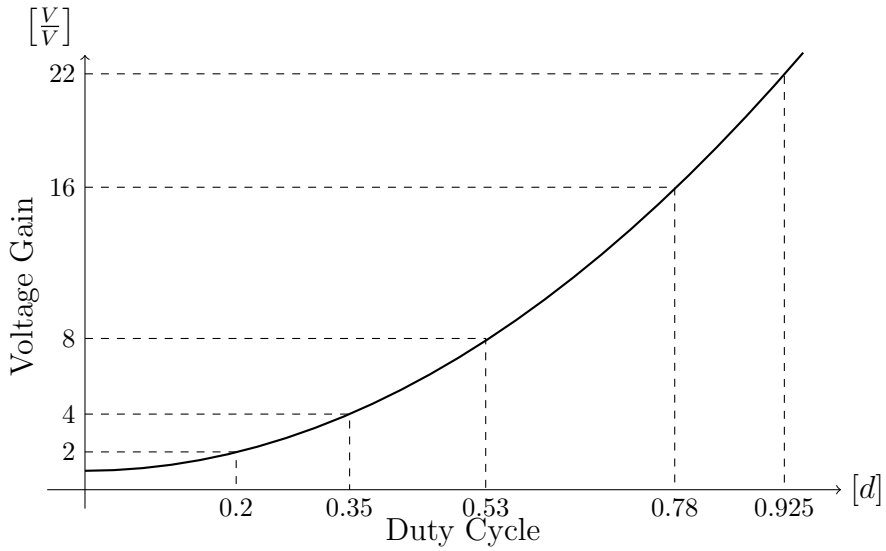


Figure 1.5: Voltage Gain in DCM versus duty cycle

In the case scenario proposed the sensitivity of the voltage gain grows at a much slower rate in comparison. To be able to maintain the output voltage of 10V with a permissible ripple of ±100mV our duty cycle can not go beyond 60.9% or below 60.3%. This translates to a resolution of 30 nano seconds, or 3 times less resolution compared to the CCM. Therefore for high gain converters, working in discontinuous mode will be prefered.

High Currents

Discontinuous conduction mode boost converters tend to have very high peak currents, defined by equation 1.5. This requires our switching elements to be able to conduct these high currents and that the inductors current ratings are not exceeded. The high current fluctuations also cause the output voltage to fluctuate as the output capacitors in a real case have an equivalent series resistance.

1.2 Multiphase boost

The multiphase boost converter is a circuit topology where the basic boost converter circuit is replicated and placed in parallel between the input and load. Each of the n "phases" is turned on at equally spaced intervals over the switching period.

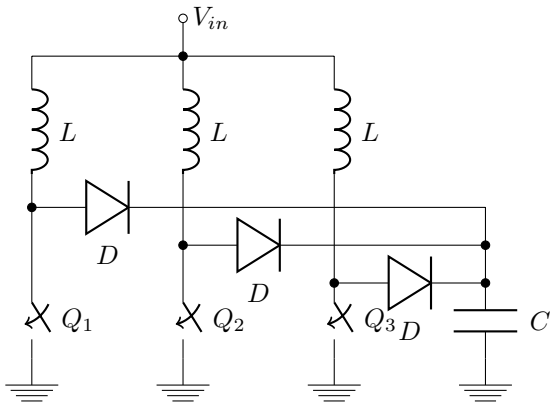


Figure 1.6: 3 phase boost topology, n=3

The equations for the standard boost converter can be applied to the multiphase converter, analyzing each phase independently.

1.2.1 General benefits

- There is a significant decrease in switching ripple.
- This type of converter can respond to load changes as quickly as if it switched at n times as fast.
- The load current is split among the n phases of the multiphase converter.

1.2.2 Current ripple

There is a significant decrease in current ripple, due to the increased effective frequency. As one inductor delivers current equally spaced throughout the switching, the decrease in current in one inductor is compensated by that of the next phase. Perfect compensation occurs at any time that n times the duty cycle is an integer, this is graphically explained in figure 1.7.

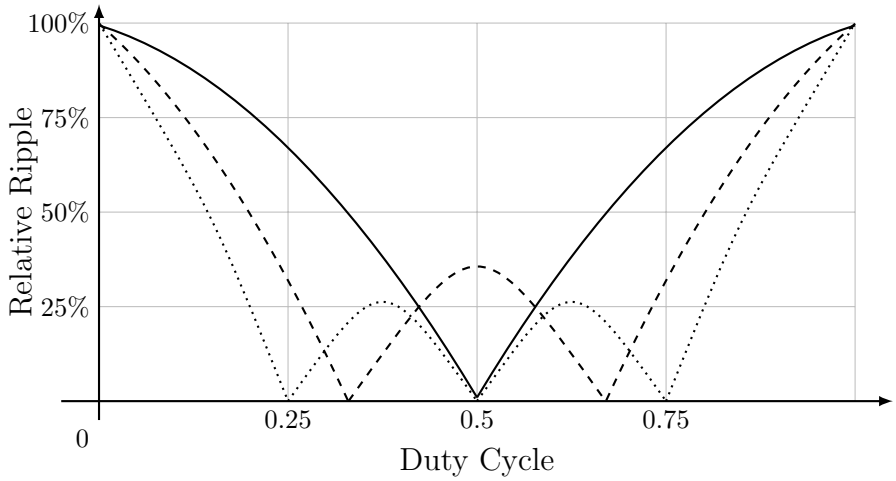


Figure 1.7: Relative current ripple of multiphase converter: n=[2,3,4]

The solid black line is a 2-phase system, the dashed line a 3-phase system and the dotted line a 4 phase system. As can be seen in figure 1.7, the switching ripple goes to 0 at multiples of $\frac{1}{n}$, being n the number of phases. The rate at which the inductor current is increasing in the phases which are switched on exactly matches the rate at which it is decreasing in the phases which are switched off. The compensation can be seen in time in figure 1.8.

1.2.3 Timing

The Timing for the circuit in figure 1.6 is depicted in figure 1.8. The switches are all switching at a 50% duty cycle. I_C is the sum of all the inductor currents.

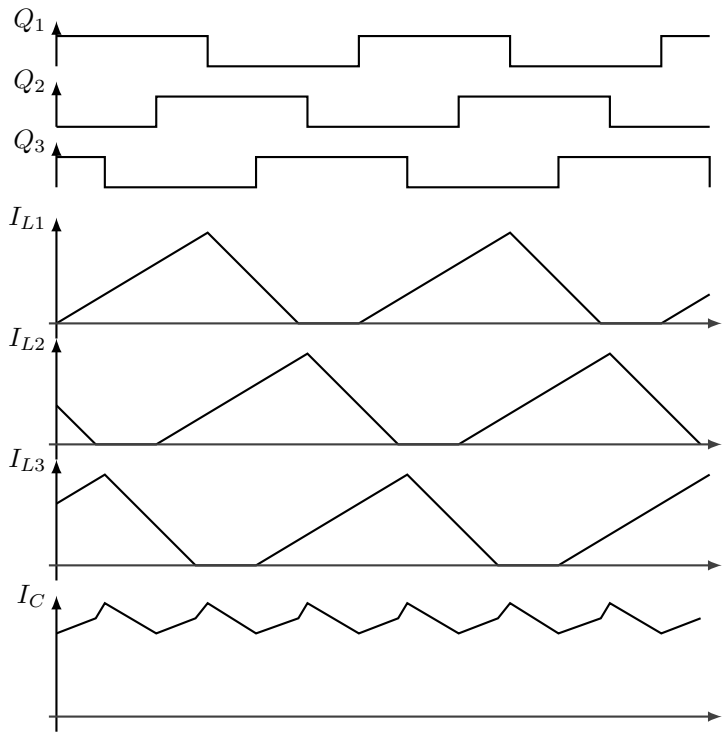


Figure 1.8: Timing of DCM in 3-Phase Boost converter

1.2.4 Current sharing

Incrementing the phases can be motivated by a desire to increase the output current or to reduce the current peaks within the circuit. For a given output current, I_{out}, adding multiple phases allows us to split the current necessities of each phase. If we have a look at equation 1.9 from the standard boost converter working in discontinuous conduction mode. Reducing the output current would allow us to increase the inductance used to maintain the same voltage gain. An increase in inductance reduces our peak current, I_{peak}, defined by equation 1.5.

Multiple phases in continuous conduction mode allow us to reduce to base current in the inductors. One of the dangers of working in CCM is to saturate the inductors.

1.2.5 Single/Multiple phase comparison

The following simulation has the parameters listed in table 1.1.

Parameter	Single Phase	Three Phase
Load current	0.5 A	0.5 A
Source Voltage	1 V	1 V
Inductance	680nH	2040nH
Output Capacitance	330μF	330μF
Duty cycle	60%	60%
Switching frequency	100kHz	100kHz

Table 1.1: Simulation parameters for single versus multiple phase comparison

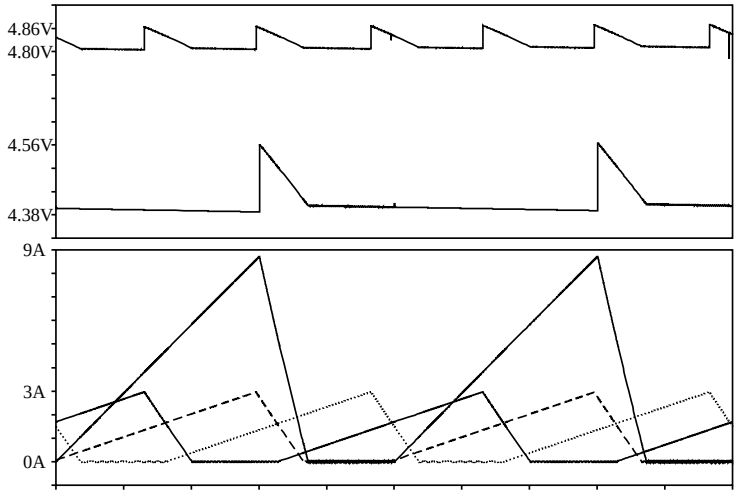


Figure 1.9: 3-Phase versus 1-Phase Boost simulation

As can be seen from the simulation plot in figure 1.9, we have managed to reduce the current requirements of components in general with the multiphase boost. The current flowing through the inductors in the multiphase system is reduced by the multiplier $\frac{1}{n}$, being n the number of phases. With the same output capacitor the ripple voltage seen has reduced by the same multiplier, being 180mV in the single phase system to 60mV in the three phase system.

With multiphase converters we have relaxed the current requirements, yet the instability in attempting to achieve high voltage gains still remains.

1.3 Tapped Boost

The tapped boost topology spawns off from a merging of the standard boost converter and the fly back converter. A standard fly back converter only takes advantage of fly back voltage produced at the secondary side, the resulting merged topology stacks secondary-winding fly back voltage on top of the input voltage and the primary-winding fly back voltage.

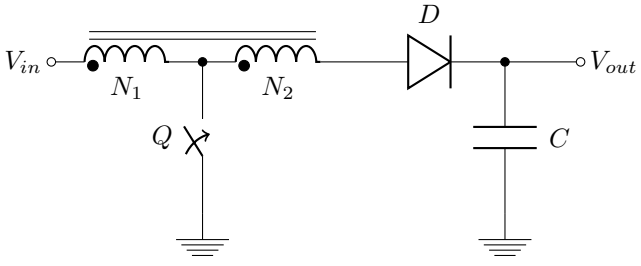


Figure 1.10: Tapped inductor topology

The transformer provides the following advantages:

- Higher attainable output voltage
- Lower operating duty cycle
- Lower voltage on the switching element

1.3.1 Circuit analysis

The tapped boost topology operates similar to the standard boost topology, with the added benefit of scaling up the output voltage by the transformer ratio.

Figure 1.11 shows the a coupled inductor model which we will use to derive further equations.

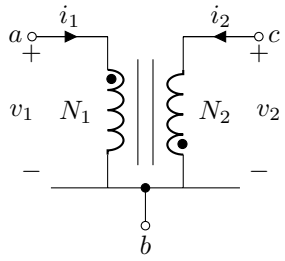


Figure 1.11: Cumulatively coupled tapped inductor

Between terminals a and c is the total inductance, L_{TOT}. In a cumulatively coupled series inductor, the voltage drops across each inductor is given as:

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \mathbf{L} \cdot \frac{d}{\delta t} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \tag{1.11}$$

$$\text{Where, } \mathbf{L} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \tag{1.12}$$

L_{11} and L_{22} are self inductances of the coupled inductors labeled N_1 and N_2, respectively. L_{12} and L_{21} are the mutual inductances of these inductors, they depend on the geometrical arrangement of the coupled inductors and can be proven to be the same value. The mutual inductance, being the same for both inductors, is given the constant M. The mutual inductance has a relationship with the coupling coefficient, k. The coupling coefficient is always between 1 and 0, and is a convenient way to specify the relationship between a certain orientation of inductor with arbitrary inductance.

$$M = k \cdot \sqrt{L_{11} L_{22}} \tag{1.13}$$

The mutual inductance can have a negative sign if the dots have different positions. The governing rule is that the induced voltage on a coupled coil has the same direction relative to its dot as the inducing current has to its own dot on the coupled counterpart. In figure 1.11, i_1 enters its inductor at the dot, meaning that the induced voltage will be negative with respect to v_2, therefore in our case M is negative.

Considering the current entering from a, i_1, as the source current and therefore positive, $i_2 = -i_1$. Rewriting our voltage drops over the inductors:

$$\mathbf{L} = \begin{bmatrix} L_{11} & M \\ M & L_{22} \end{bmatrix} \tag{1.14}$$

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \mathbf{L} \cdot \frac{d}{\delta t} \begin{bmatrix} i_1(t) \\ -i_1(t) \end{bmatrix} \tag{1.15}$$

$$v_1(t) = L_{11}\frac{\delta i_1(t)}{\delta t} - M\frac{\delta i_1(t)}{\delta t} = (L_{11} - M)\frac{\delta i_1(t)}{\delta t}$$

$$v_2(t) = M\frac{\delta i_1(t)}{\delta t} - L_{22}\frac{\delta i_1(t)}{\delta t} = (M - L_{22})\frac{\delta i_1(t)}{\delta t}$$

$$v_{a-c} = v_1 - v_2 = (L_{11} - M - M + L_{22})\frac{\delta i_1(t)}{\delta t}$$

$$v_{a-c} = L_{TOT}\frac{\delta i_1(t)}{\delta t} = (L_{11} + L_{22} - 2M)\frac{\delta i_1(t)}{\delta t}$$

$$L_{TOT} = L_{11} + L_{22} - 2M \tag{1.16}$$

From now on we will consider the coupling coefficient to be 1, ideal coupling, and the mutual inductance, M, is negative.

When the switch, Q, is turned on, the primary winding, N_1, of the transformer is subject to the input voltage. The diode, D, is reverse biased and therefore no current flows through the secondary winding, N_2. Although no current flows through the secondary winding, due to the magnetic induction from the primary, a voltage develops in the secondary.

$$v_1(t) = L_{11}\frac{\delta i_1(t)}{\delta t} + M\frac{\delta \cdot 0}{\delta t} \tag{1.17}$$

$$= L_{11}\frac{\delta i_1(t)}{\delta t} = V_{in} \tag{1.18}$$

$$v_2(t) = M\frac{\delta i_1(t)}{\delta t} + L_{22}\frac{\delta \cdot 0}{\delta t} \tag{1.19}$$

$$= (\sqrt{L_{11}L_{22}})\frac{\delta i_1(t)}{\delta t} = M\frac{\delta i_1(t)}{\delta t} \tag{1.20}$$

$$= \frac{M}{L_{11}}v_1(t) = \frac{\sqrt{L_{11}L_{22}}}{L_{11}}V_{in} \tag{1.21}$$

We can extend the relationship defined in equation 1.21 between the voltages to a more common practice such as number of turns. As is indicated by the names of the inductors in figure 1.11, L_{11} is made of N_1 turns and L_{22} is made from N_2 turns of a coil that is coupled for example by a toroid structure.

Toroid self-inductnace

To calculate the self-inductnace of a toroid which consists of N turns and has a rectangular cross section, with inner radius a, outer radius b, and height h as shown in figure 1.12:

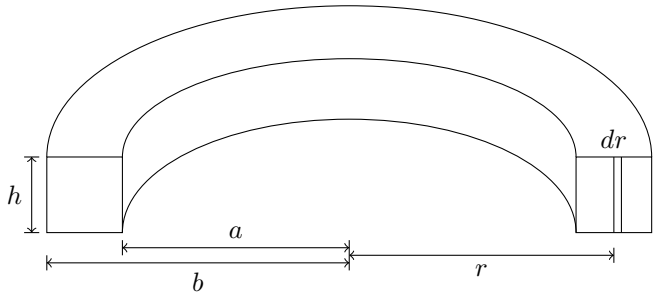


Figure 1.12: Toroid size definitions

We need to start off by calculating the magnetic flux through one turn of the toroid, Φ_B.

According to Ampere's circuital Law, the magnetic field is given by:

$$\oint_C B \cdot dl = \mu_0 \int\int_S J_f \cdot dS \tag{1.22}$$

- $\oint_C B \cdot dl$ is the closed line integral around the closed curve C, in our case the circumference of our toroid.
- B is the magnetic field measured in Tesla's, to determine the self-inductance we will assume a constant magnetic field.
- J_f is the free current density through the surface S enclosed by the curve C, in our case every turn by the current flowing through the wire contributes to the total enclosed current, $N \cdot I$.

$$B = \frac{\mu_0 \cdot N \cdot I}{2 \cdot \pi \cdot r} \tag{1.23}$$

The magnetic flux through one turn of the toroid may be obtained by integrating over the rectangular cross section with $dA = hdr$ as the differential area element:

$$\Phi_B = \int\int B \cdot dA = \frac{\mu_0 \cdot N \cdot I}{2 \cdot \pi} \cdot \int_{r=a}^{r=b} \frac{h}{r} dr \tag{1.24}$$

$$= \frac{\mu_0 \cdot N \cdot I \cdot h}{2 \cdot \pi} ln\left(\frac{b}{a}\right) \tag{1.25}$$

The total flux is $N \cdot \Phi_B$. Therefore, the self inductance is:

$$L = \frac{N \cdot \Phi_B}{I} = \frac{\mu_0 \cdot N^2 \cdot h}{2 \cdot \pi} ln\left(\frac{b}{a}\right) \tag{1.26}$$

Coupled inductance to turns relation

From equation 1.26 we see that the self inductance, L, depends only on geometrical factors which in a given coupled inductance are fix. Regrouping all the constant parameters into one I will call $A_0 = \frac{\mu_0 \cdot h}{2 \cdot \pi} ln\left(\frac{b}{a}\right)$. Our inductance can be now calculated as:

$$L = N^2 \cdot A_0 \tag{1.27}$$

Referring back to equation 1.21, to be able to define the voltage relationship between primary and secondary winding as a function of turns we will calculate the self-inductances as a function of their turns.

$$\begin{aligned} v_2(t) &= \frac{\sqrt{L_{11} L_{22}}}{L_{11}} v_1(t) \\ &= \frac{\sqrt{A_0 \cdot N_1^2 \cdot A_0 \cdot N_2^2}}{A_0 \cdot N_1^2} v_1(t) \\ v_2(t) &= \frac{N_2}{N_1} v_1(t) \end{aligned}$$

So, in the first phase, when switch Q is closed the primary coil is at V_{in} and the secondary coil at $\frac{N_2}{N_1} V_{in}$.

Inductance as a function of transformer ratio

If we don't know the primary inductance of a tapped inductor but do know the turn ratio a total inductance we can deduce the inductance seen on the primary side.

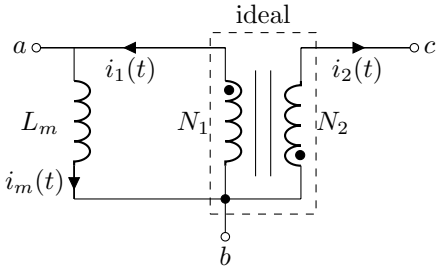


Figure 1.13: Cumulatively coupled tapped inductor equivalent circuit

Using Kirchoff's current laws:

$$i_m(t) - i_1(t) = i_2(t) \tag{1.28}$$

$$i_1(t) = i_2(t) \cdot \frac{N_2}{N_1} \tag{1.29}$$

$$i_m(t) = i_2(t) \left(\frac{N_1 + N_2}{N_1} \right) \tag{1.30}$$

The voltage across the equivalent primary inductance, L_m, is:

$$v_{a-b} = L_m \frac{\delta i_m(t)}{\delta t} \tag{1.31}$$

The primary voltage to the secondary voltage was related by number of turns from equation 1.28, therefore the voltage across the N_2 winding is:

$$v_{b-c} = \frac{N_2}{N_1} \cdot v_{a-b} \tag{1.32}$$

$$= \frac{N_2}{N_1} \cdot L_m \frac{\delta i_m(t)}{\delta t} \tag{1.33}$$

$$= \frac{N_1 N_2 + N_2^2}{N_1^2} \cdot L_m \frac{\delta i_2(t)}{\delta t} \tag{1.34}$$

So by considering the voltage drop over the series inductor:

$$v_{a-c} = v_{a-b} + v_{b-c} \tag{1.35}$$

$$L_{TOT} \frac{\delta i_2(t)}{\delta t} = \left[\left(\frac{N_2}{N_1} + 1 \right) \cdot \left(\frac{N_1 + N_2}{N_1} \right) \right] L_m \frac{\delta i_2(t)}{\delta t} \tag{1.36}$$

$$L_{TOT} = \left(\frac{N_2 + N_1}{N_1} \right)^2 \cdot L_m \tag{1.37}$$

$$L_m = \left(\frac{N_1}{N_2 + N_1} \right)^2 \cdot L_{TOT} \tag{1.38}$$

To simplify the expressions deduced later on, we will express the turns ratio, N, as:

$$N = \frac{N_1 + N_2}{N_1} \tag{1.39}$$

1.3.2 Waveforms

The peak current, I_{peak}, which the primary inductor reaches is given by the primary self-inductance, L_{11}, or the equivalent primary inductance, L_m.

$$I_{peak} = V_{in} \frac{d \cdot T}{L_{11}} = V_{in} \frac{d \cdot T}{L_m} \tag{1.40}$$

When the switch, Q, is turned off, current flows from the input, through the primary and secondary windings, through the diode, D, to the output. The current descending slope is defined by the total inductance of the series coupled inductances.

$$\frac{\delta i}{\delta t} = \frac{V_{out} - V_{in}}{L_{TOT}} \tag{1.41}$$

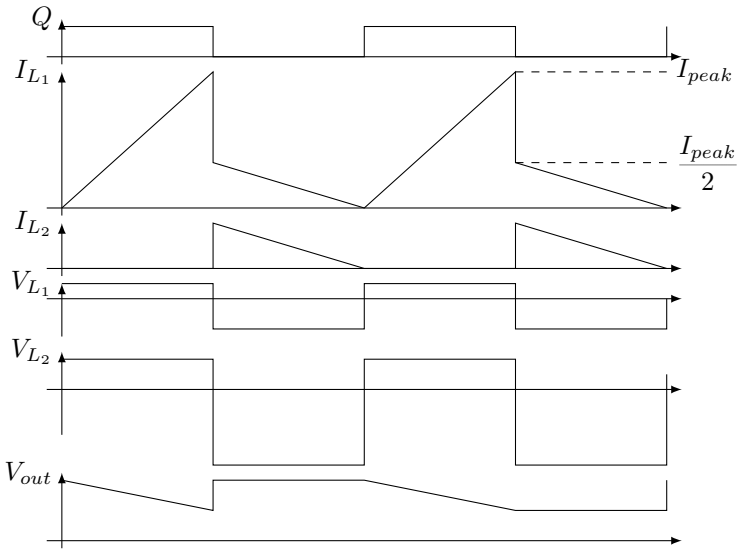


Figure 1.14: Switching waveforms of tapped boost converter

From figure 1.14, it can be seen that the downward current ramp starts at a current defined by the input current peak and the coupled inductor ratio.

$$\Delta I_{down} = \frac{\Delta I_{up}}{N} \tag{1.42}$$

Equating the two current equations at the boundary between continuous and discontinuous conduction mode.

$$\frac{V_{out} - V_{in}}{L_{TOT}}(1-d)\cdot T = \frac{V_{in}}{N}\frac{d\cdot T}{L_m} \tag{1.43}$$

$$\frac{V_{out} - V_{in}}{L_{TOT}}(1-d) = \frac{V_{in}\cdot N^2}{N}\frac{d}{L_{TOT}} \tag{1.44}$$

$$\frac{V_{out} - V_{in}}{V_{in}} = \frac{N\cdot d}{(1-d)} = \frac{V_{out}}{V_{in}} - 1 \tag{1.45}$$

Chapter 2

Deriving Classical Boost Equations

2.1 Introduction

In the following sections I will present an ideal study of the classical boost topology. I will derive the mathematical relationships which allow us to define the transfer function of the circuit presented.

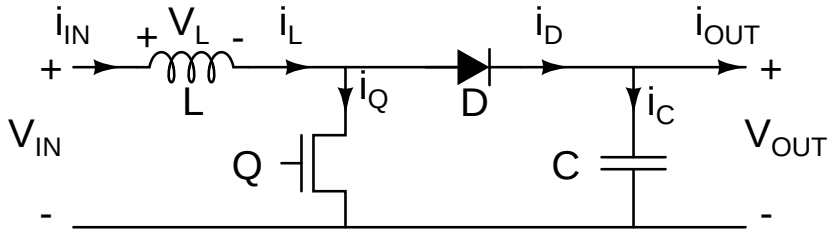


Figure 2.1: Classical boost topology component layout

Before analyzing the circuit it must be assumed that the circuit in figure 2.1 forms part of a feedback loop. This feedback loop typically has as input the circuits output voltage, V_{out}, and as output it controls a switching element, in the figure represented as Q. Ideally, there are two states of interest; one when the switching element, Q, acts as a short circuit and the other when it acts as an open circuit. The first state we will call *Time on* and the second *Time off*. The input voltage, V_{in}, is assumed to be positive following the sign convention and during our time of analysis, constant. The output voltage, V_{out}, is also assumed to be positive following the sign convention. All components are assumed ideal unless otherwise stated.

2.2 Time on

When Q is turned on for a time t_{on}, D is reverse-biased and current is fed into our inductor L. The circuit in this state is depicted in figure 2.2.

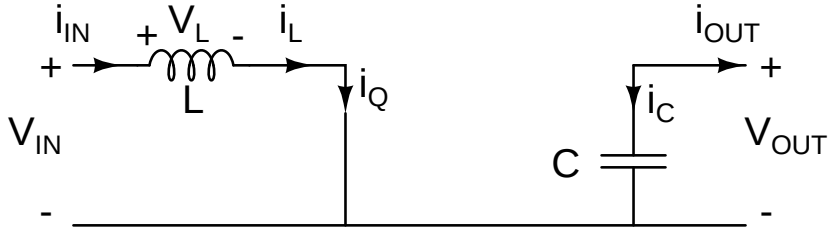


Figure 2.2: Classical Boost circuit - Time on

The original circuit can momentarily be broken up into two sub circuits which we can analyze independently. We shall refer to the sub circuit formed by the input voltage,V_{in}, the inductor, L, and the switching

element (in this state considered a short circuit to ground), Q, as the input circuit. Subsequently, the circuit formed by the output voltage, V_{out}, and the capacitor, C, shall be referred to as the output circuit.

2.2.1 Output Circuit

The output is solely supported by the capacitor C during this time, t_{on}. We can write the following equations which will help us define the output in time.

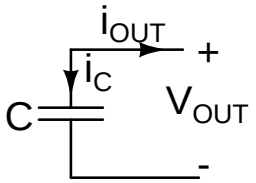


Figure 2.3: Simplified Output circuit-Time on

$$i_c(t) = \frac{d[q]}{dt} = C\frac{d[v_c]}{dt} \tag{2.1}$$

$$q(t) = \int_{-\infty}^{t} i_c(\tau)d\tau = q(0) + \int_{0}^{t} i_c(\tau)d\tau \tag{2.2}$$

$$v_c(t) = \frac{q(t)}{C} \tag{2.3}$$

The energy absorbed by our circuit during our time t_{on} will cause a voltage drop in our capacitor. Energy is the integral of power over time so lets start by calculating the power.

$$p(t) = v(t)i(t) = Cv(t)\frac{d[v(t)]}{dt} \tag{2.4}$$

$$p(t)dt = Cv(t)d[v(t)] \tag{2.5}$$

$$\int_{t_{on}} p(t)dt = \frac{1}{2}Cv^2(t) \tag{2.6}$$

Unless we have an expression for $p(t)$, being consumed by an external circuit hooked up, we will consider average power consumption, p_{avg}.

$$\Delta E_{C_{on}} = p_{avg} \cdot t_{on} \tag{2.7}$$

Which, in interest of defining characteristics of a power supply, we can translate to a voltage variation (or simply voltage drop) in the capacitor and therefore at the output as well.

$$\Delta V_c = \sqrt{(2 \cdot \Delta E_C)/C} \tag{2.8}$$

Equation 2.8 derives from $W = \frac{1}{2}CV^2$, where work, W, is understood as the energy stored in the capacitor and C is the capacitance.

2.2.2 Input Circuit

During the t_{on} phase the input of the circuit charges up the inductor, L.

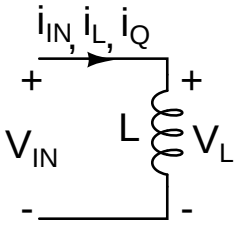


Figure 2.4: Simplified Input circuit-Time on

$$V_L(t) = L\frac{d}{dt}i_L \tag{2.9}$$

$$i_L(t) = \frac{1}{L}\int_{-\infty}^{t_{on}} V_L(\tau)d\tau \tag{2.10}$$

$$= i_L(0) + \frac{1}{L}\int_{0}^{t_{on}} V_L(\tau)d\tau \tag{2.11}$$

As we are assuming a steady state, in general we are only interested in deriving the change in current acquired by this phase.

$$\Delta i_L = \frac{1}{L}\int_{0}^{t_{on}} V_{in}(\tau)d\tau \tag{2.12}$$

As at our moment of observation V_{in} is assumed to be constant leading to:

$$\Delta i_L = \frac{V_{in}}{L}\int_0^{t_{on}} d\tau \tag{2.13}$$

$$= \frac{V_{in}t_{on}}{L} \tag{2.14}$$

The power during our time t_{on} is the energy that the circuit has acquired.

$$p(t) = v(t)i(t) = L\frac{d[i(t)]}{dt}i(t) \tag{2.15}$$

$$p(t)dt = Li(t)d[i(t)] \tag{2.16}$$

$$\int p(t)dt = L\int i(t)d[i(t)] \tag{2.17}$$

$$= \frac{Li^2(t)}{2} \tag{2.18}$$

In discontinuous conduction mode, DCM, we are interested in the change of energy:

$$\Delta E_{L_{on}} = \int_{t_{on}} p(t)dt \tag{2.19}$$

$$= \frac{L\Delta i_L^2}{2} = \frac{V_{in}^2 t_{on}^2}{2L} \tag{2.20}$$

In continuous conduction mode, CCM, we are interested in the absolute energy:

$$E_{L_{on}} = \int_{-\infty}^{0} p(t)dt + \int_0^{t_{on}} p(t)dt \tag{2.21}$$

$$= \frac{L}{2}\left[i_L(0)^2 + \Delta i_L^2\right] \tag{2.22}$$

$$= \frac{L\cdot i_L(0)^2}{2} + \frac{V_{in}^2 t_{on}^2}{2L} \tag{2.23}$$

2.3 Time off

Q is turned off for a time t_{off}, D is now forward-biased and current is fed from the input, V_{in} through the inductor, L, to the capacitor C and output. The circuit at this moment is:

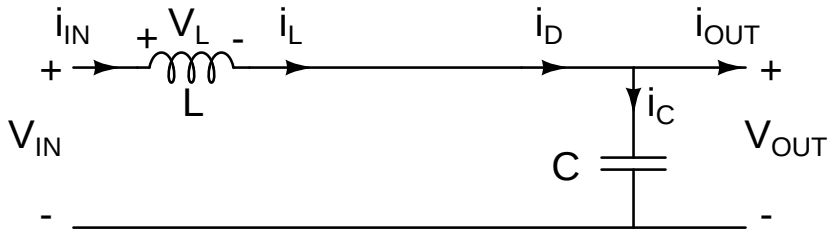


Figure 2.5: Classical Boost circuit - Time off

The current in an inductor cannot change instantaneously, so it reverses its voltage in an attempt to maintain the current constant.

In a steady state and considering discontinuous conduction mode, DCM, the inductor transfers all of its energy to the capacitor, C, and output. In a steady state and considering current conduction mode, CCM, the inductor only transfers all the energy acquired during the t_{on} phase to the capacitor, C, and output.

$|\Delta E_{L_{on}}| = \left|\Delta E_{L_{off}}\right|$ The current flowing through the inductor also flows through the input voltage source, contributing power during this time, $t_{off} \rightarrow p_{V_{in}} = V_{in}\cdot i_L(t)$.

2.3.1 Discontinuous Conduction Mode

The inductor current will vary through time depending on the load. If we sketch the current through the inductor in several cases we will see how the definition of the energy from the input source is not as trivial as we may have thought.

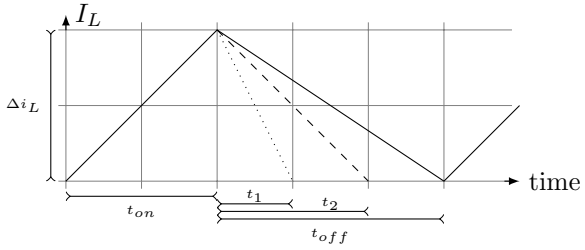


Figure 2.6: Current in inductor in DCM with different loads

We need to define a new time which defines the time required for the inductor to transfer all of its current to the output, in other words descends to zero. We will name it t_r. During this time, $t_r = \{t_1, t_2, t_{off}\}$, we will have an average current of $\frac{\Delta i_L}{2}$. Energy from the input

$$\Delta E_{IN_{off}} = V_{in} \cdot \frac{\Delta i_L}{2} \cdot t_r \tag{2.24}$$

As this phase is the only one contributing energy to the output, assuming a steady state, it must account for the energy drawn during both phases.

$$\Delta E_{L_{off}} + \Delta E_{IN_{off}} = \Delta E_{C_{off}} + \Delta E_{OUT_{off}} \tag{2.25}$$

Where $\Delta E_{L_{off}} = \Delta E_{L_{on}}$ as similarly $\Delta E_{C_{off}}$ represents a charging of the capacitor to compensate for the energy lost during the t_{on} phase, $|\Delta E_{C_{on}}| = \left|\Delta E_{C_{off}}\right|$.

$\Delta E_{OUT_{off}}$ is the energy consumed during the t_{off} phase by the external circuit. Substituting equations (2.23), (2.24) and (2.7) into 2.25 and considering the energy extracted during the off phase similarly as in equation (2.7).

$$\frac{L \cdot \Delta i_L^2}{2} + V_{in} \cdot \frac{\Delta i_L}{2} \cdot t_r = p_{avg} \cdot t_{on} + p_{avg} \cdot t_{off} = p_{avg} \cdot T \tag{2.26}$$

Leaving the prior as a function of the input voltage, average power and times with the help of equation 2.14.

$$\frac{V_{in}^2 t_{on}^2}{2L} + V_{in} \cdot \frac{V_{in} t_{on}}{2L} \cdot t_r = p_{avg} \cdot T \tag{2.27}$$

$$\frac{V_{in}^2 t_{on}}{2L} \cdot (t_{on} + t_r) = p_{avg} \cdot T \tag{2.28}$$

p_{avg} is the average output power drawn. If we model our load to be basically resistive; $p_{avg} = \frac{V_{out}^2}{R}$ Rearranging the equations:

$$\frac{V_{in}^2 t_{on}}{2L} \cdot (t_{on} + t_r) = \frac{V_{out}^2}{R} \cdot T \tag{2.29}$$

$$\sqrt{\frac{R t_{on}}{2TL} \cdot (t_{on} + t_r)} = \frac{V_{out}}{V_{in}} \tag{2.30}$$

2.3.2 Continuous Conduction Mode

The inductor current is made out of two parts in the CCM. There is a steady state current base and a current ripple, while in DCM there is only the current ripple. The amount of energy absorbed during the t_{off} period will vary through time depending on the load. If we sketch the current through the inductor in several cases we will see how the definition of the energy from the input source is not as trivial as we may have thought.

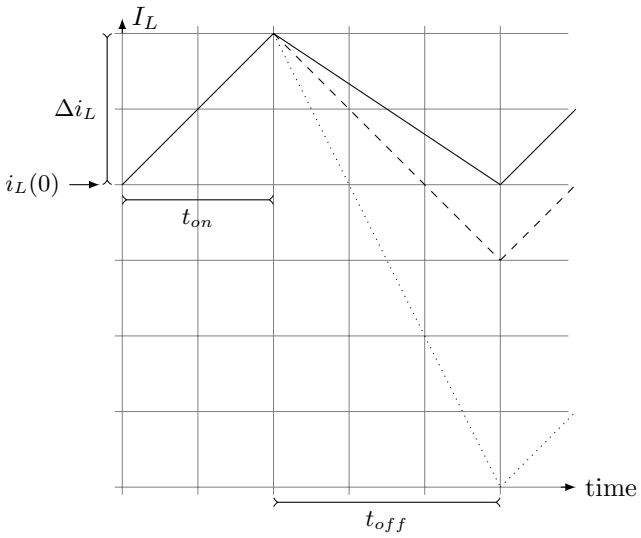


Figure 2.7: Current in inductor in CCM with different loads

As we can see from the graphic as long as the input voltage is constant, the current ramp during the t_{on} phase is also constant. If the output consumption changes our current ramp will also change decreasing the power which is being contributed by the power source and the inductor. To recover our steady state average current which is required we will need to increase the duty cycle to charge up the inductor more.

The rate at which the output current ramp will decrease is $\frac{V_{in} - V_{out}}{L}$. The worst ripple case is at the boundary between DCM and CCM.

2.3.3 Boundary equations

The boundary between continuous and discontinuous current modes in the boost converter is when $t_{on} + t_r = T$. Using this condition in equation 2.30.

$$\sqrt{\frac{Rt_{on}}{2L}} = \frac{V_{out}}{V_{in}} \tag{2.31}$$

If $t_r > t_{off}$, understanding t_r as the time required for the inductor to transfer all of its stored current to the output, there will be a remaining current in the inductor and the next cycle will start with a "base" current, different than zero. This can be provoked by an increase in power consumption by the circuit connected at the output. The control loop will adjust t_{on} at Q to maintain a constant voltage. As R or V_{in} decrease t_{on} will increase to maintain the equality. Given a constant t_r, defined by the circuit, as t_{on} increases t_{off} decreases until the point that $t_r > t_{off}$.

If we want the acquired current during t_{on} to be drained during t_r. The acquired current for the t_{on} phase is described by equation 2.14. In the t_{off} phase we have something similar, assuming V_{out} and V_{in} to be constant.

$$\Delta i_{L_{off}} = \frac{V_{out} - V_{in}}{L} \int_0^{t_r} d\tau \tag{2.32}$$

$$= \frac{(V_{out} - V_{in}) \cdot t_r}{L} \tag{2.33}$$

At the boundary $t_r = t_{off}$

$$\Delta i_{L_{off}} = \Delta i_{L_{on}}$$

If we want to stay in DCM we must make sure that the current extracted during the t_{off} phase be larger than that acquired in the t_{on} phase. Logically then extra current required will need to come from another

source, this is the output capacitor, and will be noted as a decrease in output voltage.

$$\frac{(V_{out} - V_{in}) \cdot t_{off}}{L} \geq \frac{V_{in} t_{on}}{L} \tag{2.34}$$

$$\frac{V_{out} - V_{in}}{V_{in}} \geq \frac{t_{on}}{t_{off}} \tag{2.35}$$

$$t_{on} + t_{off} = T$$

$$t_{on} \leq T \cdot \frac{V_{out} - V_{in}}{V_{out}} \qquad D = \frac{t_{on}}{T} \qquad \frac{V_{out}}{V_{in}} = \frac{1}{1 - D}$$

Given circuit definitions such as $V_{out_{max}}$, $V_{in_{min}}$, p_{max} and switching frequency, f, we can define the maximum size of our inductor to stay in DCM.

$$f = \frac{1}{t_{on} + t_{off}} \qquad p_{max} = \frac{V_{out_{max}}^2}{R}$$

$$L \leq \frac{(V_{out_{max}} - V_{in_{min}}) V_{in_{min}}^2}{2 \cdot V_{out_{max}} \cdot p_{max} \cdot f} \tag{2.36}$$

Now we have the basic formulas to start to design a boost converter working in DCM. If we wanted to work in CCM then we would have to consider the opposite limitations, where we need a minimum current consumption to be CCM.

$$L \geq \frac{(V_{out_{min}} - V_{in_{max}}) V_{in_{max}}^2}{2 \cdot V_{out_{min}} \cdot p_{min} \cdot f} \tag{2.37}$$

Chapter 3

Design Specifications

In this chapter I will derive or justify the parameters chosen for the design.

3.1 Input voltages

A solar cells output voltage, our input voltage, is a function of the irradiance level and temperature it is exposed to. Irradiance levels will vary depending on the inclination angle of the plane which is the solar panel. For calculation purposes we will assume that the normal of this plane is pointing towards the sun at all times and therefore a constant radiation can be assumed. Irradiance levels at the umbra (total shadow) of the earth are assumed to be too low to generate energy.

3.1.1 Voltage Characteristics

Assuming Clyde-space has expanded from the kits which CubeSat developed, I have checked the solar cells which they used in their kits. From the datasheets I have extracted the following information on voltage characteristics.

Cell Name	Company	V_{oc}	V_{mp}	V_{mp}(mV/°C)	V_{oc}(mV/°C)
BTJ	emcore	2.700 V	2.370 V	-6	-6
BTJM	emcore	2.680 V	2.325 V	-6	-6
UTJ	Spectrolab	2.665 V	2.350 V	-6.5	-5.9
XTJ	Spectrolab	2.628 V	2.333 V	-6.5	-5.9
ATJ	emcore	2.600 V	2.300 V	-5.93	-5.48
ATJM	emcore	2.575 V	2.285 V	-5.93	-5.48
ITJ	Spectrolab	2.565 V	2.270 V	-6.2	-5.9
TJ	Spectrolab	2.545 V	2.275 V	-6.7	-6.4
DJ	Spectrolab	2.360 V	2.085 V	-4.6	-4.2
SJ	Spectrolab	1.025 V	0.900 V	-1.9	-1.8

Table 3.1: Voltage Characteristics of solar panels used in space

Values measured with the Bare Cell exposed to AM0 (135.3 mW/cm^2) at 28°C

The irradiance levels at the Earth's distance from the Sun are about 135.3 mW/cm^2.

The table is organized with V_{oc} (open circuit voltage) decreasing. As irradiance levels decrease so does the open circuit voltage. The irradiance levels are assumed to be constant except for the transition stage into the penumbra (partial shadowing) of the earth, where we can expect a decrease of upto 15% in the open circuit voltage before reaching an uninteresting levels. From the table we can see that only the Single Junction (SJ) technology provides the lowest voltage threat, with the 15% decrease we should have energy down to 765mV.

Temperature influence

For starters I am going to use the extreme operational temperatures at which the electronics can work: -40°to 125°C

-40°C is 68°away from 28°C
125°C is 97°away from 28°C

Cell	Company	V_{oc}@-40°C	V_{oc}@125°C	V_{mp}@ -40°C	V_{mp}@125°C
BTJ	emcore	3.108 V	2.118 V	2.778 V	1.788 V
TJ	Spectrolab	2.980 V	1.924 V	2.730 V	1.625 V
SJ	Spectrolab	1.147 V	0.850 V	1.029 V	0.715 V

The actual temperature of the solar cell in space is a complex calculation but to get an idea we recur to an already formulated example [1] .

For the special case of a perfectly black, highly conductive sphere in the Solar System at a distance R from the Sun, absorbing solar radiation from one side, but radiating in all directions equally, it turns out that the temperature drops with distance from the Sun as the square root of $1/R$

$$T = 277°K \cdot \sqrt{\frac{1AU}{R}} \tag{3.1}$$

where, 1 AU is the average distance from the Earth to the Sun, 1 Astronomical Unit = 149 598 000 kilometers. T is the "characteristic temperature" at a distance R from the Sun.

For a satellite in Low Earth Orbit (LEO), up to 2000 km from the earth, the calculation resolves to a temperature of 277°K. Therefore temperature seems not to be our concerning factor on the minimum voltage case, yet it does help us resolve the maximum input voltage.

3.1.2 Input Voltage Specifications

As a operating input voltage specifications we have:

$$V_{in_{min}} = 700mV \qquad V_{in_{max}} = 3200mV$$

3.2 Maximum Power

In this section we will size the power output capabilities of the boost stage.

3.2.1 Triangular estimate

According to the SalleSat specifications, our day consists of 62 minutes. We use Cylde-Space prior mission details on similar projects as a reference. They state to expect around 2000mWh during the day from our solar panels, this is taking into account the size of our cube ($10cm \times 10cm \times 10cm$). A crude estimation of the solar radiation which we are exposed to is by a triangle.

Triangle	Reality	Quantity
Base	Time exposure	1 hour
Area	Accumulated Energy	2Wh
Height	Maximum Power peak	$\frac{1}{2} \cdot 1h \cdot$height= 2Wh height=4W

Table 3.2: Triangular power approximation

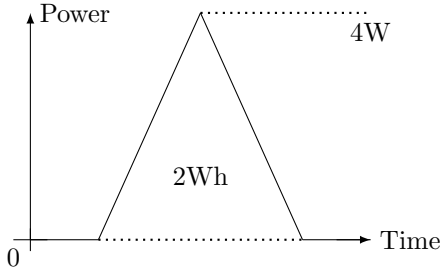


Figure 3.1: Triangular power approximation

[1] http://www.wwheaton.com/waw/mad/mad5.html

A first approximation of design specifications is to deliver a P_{max}=**4000mW**.

Available Solar Panels

I have taken into consideration several solar panel datasheets available in the cylde-space website[2]. The main manufacturers are Spectrolab (SL) and Emcore (EC) ranging from single junction solar cells to triple junction cells.

Solar Cell	Max Power / cm^2	Voltage @ Max Power	$100cm^2$ power
SL: SJ	25.7mW	0.9	2570mW
SL: DJ	29.5mW	2.085	2950mW
EC: BTJM	38mW	2.33	3800mW
SL: XTJ	40.41mW	2.333	4041mW
EC: BTJ	38.83mW	2.37	3883mW
SL: UTJ	38.3mW	2.35	3830mW
SL: ITJ	36.3mW	2.27	3630mW
EC: ATJ	37.26mW	2.3	3726mW
SL: TJ	33.89mW	2.275	3389mW
EC: ATJM	36.56mW	2.285	3656mW

Table 3.3: Available power from different solar cells

Using the data from table 3.3 we make a linear approximation, always being above the nominal values.

Vin	Pout
0.7	2.5W
2.3	4W

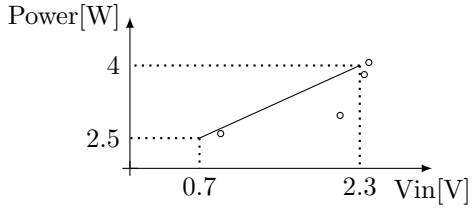


Figure 3.2: Linear approximation of available power

As seen in section 3.1.1 our input voltage can fluctuate 500mV depending on the temperature the solar cells are at.

3.3 Output Voltage

The output of the $ARLV_{MPPT}$ will branch to a Lithium-Ion Battery charger and to the *Raw-PowerBUS*. The Raw-PowerBUS is a roughly regulated power source where we will have a other Switch Mode Power Supplies (SMPS) to provide adequate voltage levels to the other electronics.

Lithium-Ion Charge Cycle

To charge a **single cell** battery:

- current is injected at a specified rate.
- the voltage per cell reaches 4.2 volts.
- voltage is maintained constant as current drops.

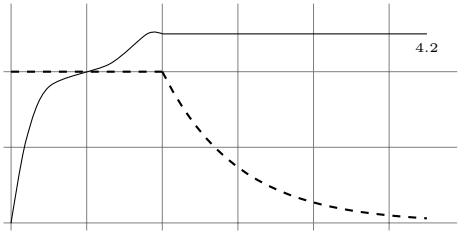


Figure 3.3: Lithium-Ion Charge Cycle

[2]www.clyde-sapce.com

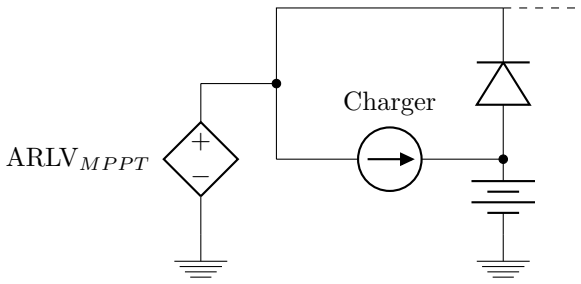


Figure 3.4: ARLV$_{MPPT}$ in system layout

The SalleSat specifies that we will have two Lithium Ion Cells connected in series. Considering that the charger has at least a 95% efficiency. Our minimum Raw-PowerBUS voltage level:

$$V_{min} \geq \frac{4.2}{0.95} + \frac{4.2}{0.95} = 8.85V$$

Our design target is no higher than 12V but in no case can we have a voltage level lower than 9V.

3.3.1 Output Voltage Specifications

As operating output voltage specifications we have:

$$V_{out_{min}} = 9V \qquad V_{out_{max}} = 12V$$

3.3.2 Voltage/Current ripple

As discussed previously, our target voltage is to have 12 Volts DC with in no case having a voltage below 9V. This leads to a calculation of **Maximum Ripple** Voltage:

$$\begin{aligned} V_{Ripple} \leq & \frac{12-9}{2} = 1.5Volts \\ I_{Ripple} \leq & \frac{P_{max}}{V_{Ripple}} \\ & \frac{4W}{1.5V} = 2.6\overline{6}Amps \end{aligned}$$

Obviously our design is going to try to reduce these parameters to a minimum taking into account other factors such as fiability, bandwidth *(stability)*, weight, size and efficiency. These parameters here are defined as **Absolute Maximum**.

3.3.3 Switching Frequency

Putting our Booster in context, we are going to be controlling the duty cycle of our system with a micro controller. The algorithm and hardware presented will be general, but the actual firmware and realization will be done with a Microchip Pic 8-bit micro controller, specifically the PIC16F690.

Looking into the Pulse Width Modulator section we find the formulas for calculating the frequency and resolution which we can obtain.

Limiting Factors	Limited to	Reason
Operating Frequency	8MHz	We are to work and start at low voltages. The permissible combinations of frequency and voltage below 3Volts is limited to 8MHz
Resolution	below 2% of range	Given the nature of the Voltage-Current characteristics of the solar panels we need to have a reasonable number of points to track the MPPT with a fair precision.

Table 3.4: Microchip PWM restrictions in context

With these restrictions we derive that we need at leasts 6 bits of resolution and calculation through the formula presented in the datasheet leads to:

$$\text{Maximum switching frequency} = 125\ kHz$$

3.4 Parameter Specification summary

Parameter	Design Value
P_{max}	4000mW
$V_{in_{max}}$	3.2 Volts
$V_{in_{min}}$	0.7 Volts
$V_{out_{max}}$	12 Volts
$V_{out_{min}}$	9 Volts
$V_{out_{Ripple}}$	$\leq 1.5 Volts$
f_{max}	125 kHz

Table 3.5: Parameter Specification summary

Chapter 4

Component Calculations

To drift away from the beautiful world of theory where there is a component which fits every need, this section is to get a feeling of what should be taken into account given real world components and specifications to meet. The calculations made here and components selected have been based on theoretical approximations and simulations.

4.1 Inductance

4.1.1 Introduction

The inductance is the primary element for stepping up the voltage. It accumulates energy and stores it in the form of a magnetic field. Changes in the electrical circuit connections to the inductance allow for the transformation from a magnetic field to the forms of voltage and current.

Other Parameters defining an inductor

- Maximum DC current (I_{RMS}): The maximum DC current is defined as the DC current at which the inductance falls to 90% of its nominal value or until its internal temperature rises 30°C, whichever is sooner.
- Inductance Temperature coefficient: The change in inductance per temperature change. Measured in parts per million (ppm).
- Resistance Temperature coefficient: The change in DC wire resistance per unit temperature change. Measured in parts per million (ppm).
- Currie Temperature (T_C): The temperature beyond which the core material loses its magnetic properties.
- Magnetic Saturation flux density (B_{SAT}): A core parameter which indicates the maximum flux the material can be induced to hold. At this value of flux density all magnetic domains within the core are magnetized and aligned, further alignment is not possible.
- Saturation: Saturation of an inductor occurs when the core can no longer store magnetic energy, (energy storage= $\frac{1}{2}LI^2$).

Some of the advantages of selecting a low vs. high inductor value for a given package, (core size and geometry) are given in table 4.1.

Benefits of Lower Inductor Values	Benefits of Higher Inductor Values
• Low DCR: lower DC inductor losses in windings • Fewer turns: higher DC saturation current • High di/dt – faster response to load step/dump – fewer output capacitors required for good load transient recovery	• Low ripple – lower AC inductor losses in core (flux) and windings (skin effect) – lower conduction losses in MOSFETs – lower RMS ripple current for capacitors – continuous inductor current flow over wider load range

Table 4.1: High/Low Inductance value benefits

4.1.2 Inductor for DCM

For the classical boost converter operating in discontinuous conduction mode the calculated maximum inductance to stay in DCM is:

$$L \leq \frac{(V_{out_{max}} - V_{in_{min}})V_{in_{min}}^2}{2 \cdot V_{out_{max}} \cdot p_{max} \cdot f}$$
$$L \leq \frac{(12 - 0.7)0.7^2}{2 \cdot 12 \cdot 2.5 \cdot 125 \times 10^3} = \frac{5.537}{7500 \times 10^3} = 738.3nH$$

This is the theoretical calculated value. The lower the inductance the higher our peak current.

Standardized values lead me to choose between two inductance values, 680nH or 470nH. Lets derive the theoretical peak current in these inductors.

$$I_{peak} = \frac{V_{in} t_{on}}{L} \qquad t_{on} \leq \frac{1}{f_{SW}} \cdot \frac{V_{out} - V_{in}}{V_{out}} \qquad I_{peak} = \frac{V_{in} \frac{1}{f_{SW}} \frac{V_{out} - V_{in}}{V_{out}}}{L}$$
$$I_{peak} = \frac{V_{in_{max}}(V_{out_{max}} - V_{in_{max}})}{L \cdot f_{SW} \cdot V_{out_{max}}} = \frac{4(12-4)}{L \cdot 100 \times 10^3 \cdot 12} = \frac{26.67 \times 10^{-6}}{L}$$
$$I_p(680nH) = \frac{26.67 \times 10^{-6}}{680 \times 10^{-9}} = 39.2A \qquad I_p(470nH) = \frac{26.67 \times 10^{-6}}{470 \times 10^{-9}} = 56.7A$$

These are very high current levels, we might have problems with the PCB traces having such a high current flux density. To be on the safe side, I have chosen the 680nH inductance for the proposed design.

Component Selection

Searching through what the market (Farnell Components) has to offer I have selected the following inductor.

Farnell Code	Part No.	Inductance L (μH)±20%	I rms (A)	I sat (A)	DCR (mΩ) max.
1682461	SRP1270-R68M	0.68	35	60	1.6

4.1.3 Inductor for CCM

For the classical boost converter operating in continuous current mode the calculated minimum inductance to stay in CCM is:

$$\begin{aligned} L \geq & \frac{(V_{out_{min}} - V_{in_{max}})V_{in_{max}}^2}{2 \cdot V_{out_{min}} \cdot p_{min} \cdot f} \\ \geq & \frac{(9-4) \cdot 4^2}{2 \cdot 9 \cdot p_{min} \cdot 100 \times 10^3} \\ \geq & 44.4\overline{4}\mu H \cdot \frac{1}{p_{min}} \end{aligned}$$

As shown above the minimum inductance depends on the minimum power drawn from the stage. There are several options to achieve such an inductance at the power levels that we require:

Inductances in parallel	Inductors in series	Coupled Inductors
Current is split in half, yet so is the inductance.	Inductance is summed, current remains unchanged.	Inductance extends quadratically, yet saturation currents are very low.

To minimize conduction losses most books recommend to select an inductor that produces a ripple current of 10% to 30% of full load DC current.

Component selection

RMS as well as saturation current must be above 3.6 amps and inductance must be above 90uH. Although I personally believe that working in continuous conduction mode we will not achieve the desired voltage gain factor, for proof of concept I have selected the following component for the proposed design.

Farnell Code	Part No.	μH	$I_{rms}(A)$	DCR ($m\Omega$)
1693394	2200HT-101-RC	100	5.3	61

4.2 Capacitance

4.2.1 Introduction

The design is intended for an aerospace application and therefore have certain restrictions. The output capacitor has the following requirements:

Min. °C	Max. °C	Min. Life	Desired Life	Type
-40°C	0°C	8,760 hours	40,000 hours	not electrolytic

Table 4.2: Capacitor design requirements

4.2.2 Temperature influence

Capacitance and most parameters are normally measured at 25°C.

- As temperature rises, so does the capacitance and vice-versa. In our case we will experience a maximum capacitance derating of 10% at -40°C, ≈ 3% at 0°C.
- The DC leakage current is also affected by temperature. At 0°C we have a multiplier of 0.7 and at -40°C we have 0.3 of the rated DC leakage current.
- The working voltage only requires a derating at temperatures above 85°C.

- Reverse voltage; Although Tantalum are polar capacitors, some degree of transient voltage reversal is permissible. They should not be operated continuously in this region. At 25°C a 15% of the rated voltage is specified, decreasing with temperature increase.
- ESR (Equivalent series resistance): The ESR tested at a frequency of 100kHz is affected by temperature with a multiplier of 1.5 at 0°C and 2 at -40°C.

4.2.3 Reliability prediction

Capacitor failure may be induced by exceeding the rated conditions of forward DC voltage, reverse DC voltage, surge voltage, surge current, power dissipation, or temperature. In an application note of Kemet capacitors failure rate is conventionally expressed in units of percent per thousand hours.

For manufacturing series not covered by military specifications, it is demonstrated that average failure rate for all commercial series is between .1 and 1%/Khr at standard conditions and 60% confidence after 2,000 hours testing, +85°C, and rated voltage and ≤ 1 ohm total series resistance.

According to a table of Kemet the failure rate to circuit impedance:

Circuit Impedance (multiplying factors)	0.1	0.2	0.4	0.6	0.8	1.0	2.0	≥ 3
Failure Rate Improvement (ohms/volt)	1.0	0.8	0.6	0.4	0.3	0.2	0.1	0.07

Table 4.3: Capacitor failure rate vs circuit impedance

To calculate the failure rate multiplier dependent on operating temperature and applied voltage ratio they present a Reliability Nomograph.

4.2.4 Current Limitation

At frequencies in the 10kHz to several hundred kilohertz range, the power dissipation becomes the limiting factor. The following formula gives the maximum permissible ripple current for a sinusoidal wave form:

$$I_{rms} = \sqrt{\frac{P_{max}}{ESR}} \tag{4.1}$$

Power dissipation limits calculated for the most popular surface mount types of solid tantalum capacitors are listed in table 4.4:

Case Size	A	B	C	D	E
Maximum Power @ + 25°C(Watts)	0.075	0.085	0.110	0.150	0.165

Table 4.4: Tantalum capacitor power dissipation limits

4.2.5 Output capacitor design

The reliability calculations applied to our circuit for the output capacitor.

$$P = \frac{V^2}{R} \qquad \frac{\Omega}{V} \rightarrow \frac{V^2}{V \cdot P} = \frac{V_{min}}{P_{max}} = \frac{9V}{4W} = 2.25$$

Our failure rate improvement factor is of 0.1.

Assuming an operating voltage of 12V, I am going to evaluate the difference between a 16V, 20V or 25V tantalum. The Nomograph, reaching a minimum of 25°C, returns the following adjusted failure rate estimates.

Rated Voltage	16V	20V	25V
Failure Rate multiplying factor	2×10^{-5}	2.5×10^{-6}	4×10^{-7}

Failure rate

Given the available capacitance values at the rated voltages in the market, I propose 4 capacitors in parallel with capacitors rated at 20V and half as many with capacitors rated at 16V to reach the desired capacitance. Capacitors in parallel change the impedance failure rate improvement as the impedance seen by each is lowered by the source of energy stored in the other capacitors. Adjusting our prior calculation of 2.25 ohms/volt;

Voltage Rating	Calculation	FR improvement Factor
20V	$2.25/4 = 0.56 \rightarrow$	0.5
16V	$2.25/2 = 1.12 \rightarrow$	0.2

Considering the system to be functional only with all capacitors operational, the calculated failure rate is:

Voltage Rating	Calculation	FR 10,000 hours	FR 50,000 hours
20V	$1\%/khr \cdot 2.5 \times 10^{-6} \cdot 0.5 = 1.25 \times 10^{-8}$	1.25×10^{-7}	6.25×10^{-7}
16V	$1\%/khr \cdot 2 \times 10^{-5} \cdot 0.2 = 4 \times 10^{-8}$	4×10^{-7}	2×10^{-6}

Taking into account that the probability of any one capacitor failing with twice the number of capacitors approximately doubles. I conclude that in our working environment, the failure rate for both are approximately the same and failure rate is not a parameter of decisive weight.

Current Limitation

$$I_{rms_{max}} = 3 \cdot \frac{V_{min}}{p_{max}} = 3 \cdot 9/4 \approx 1.4A$$

$$ESR_{@-40} = 2 \cdot ESR_{@+25}$$

$$I_{rms} = \sqrt{\frac{P_{max}}{2 \cdot ESR}} \qquad \frac{0.15}{2 \cdot (1.4A)^2} = ESR_{max} \leq 38m\Omega$$

SMPS recommendations

For SMPS applications at least a 30% voltage derating is recommended and up to 70% if current is not limited by a series resistance. 16V voltage rating does not satisfy the minimum derating and therefore 20V capacitors will be selected.

Component selection

Farnell Code	Capacitance	Voltage Rating	Qty
1135212	100μF	20 V	4

4.2.6 Input capacitor design

Why would we need an input capacitor? The discontinuous current mode Boost topology provoques current ramps which our input source may not be able to handle. If we add capacitors, these fluctuations will not be noticed so drastically at the input as the capacitors will act as a low pass filter. Remembering that the input source is a solar panel, modeled as a current source with series and shunt resistances, we would like to maintain the voltage variations, at the source, below our minimum step voltage for the MPPT tracking. This is dependent on our PWM step. In our best case scenario, we will be working at 8MHz which allows for a resolution of 6 bits. At the lowest voltage (0.7 Volts) we would aim for a voltage ripple below 11mV.

Power source model

Our current source has a series resistance which we will approximate for (Voc - Vmpp) /(Impp· 2.5) , the factor 2.5 is the proportional factor which corrects the error made by this approximation.

Cell Name	Company	V_{oc}	V_{mp}	P_{mpp}	R_s $100cm^2$
BTJ	emcore	2.700 V	2.370 V	38.83mW	$80m\Omega$
BTJM	emcore	2.680 V	2.325 V	38mW	$87m\Omega$
UTJ	Spectrolab	2.665 V	2.350 V	38.3mW	$77m\Omega$
XTJ	Spectrolab	2.628 V	2.333 V	40.41mW	$68m\Omega$
ATJ	emcore	2.600 V	2.300 V	37.26mW	$74m\Omega$
ATJM	emcore	2.575 V	2.285 V	36.56mW	$73m\Omega$
ITJ	Spectrolab	2.565 V	2.270 V	36.3mW	$74m\Omega$
TJ	Spectrolab	2.545 V	2.275 V	33.89mW	$73m\Omega$
DJ	Spectrolab	2.360 V	2.085 V	29.5mW	$77m\Omega$
SJ	Spectrolab	1.025 V	0.900 V	25.7mW	$18m\Omega$

Table 4.5: Calculated equivalent series resistance of available solar cells

Our boost converter is considering the input as a voltage source when it actually is best modeled as a current source. The input capacitor will be charged to the open-circuit voltage. When the boost converter demands current, they will add the additional transient current to charge up the inductor. This will result in a decrease of their voltage which will need to recover before the next cycle begins.

component selection

After several simulations the selected component is:

Farnell Code	Capacitance	Voltage Rating	ESR ($m\Omega$)
9229604	220μF	10 V	18

4.3 Diode

4.3.1 Introduction

Within the diode family rectifiers are the largest class. One talks about rectifiers, if the specified current is above 0.5 A. Below 0.5 A one normally talks about diodes. Rectifiers are primarily used, as their name already indicates, for conducting current in one direction and blocking in the other.

Within rectifiers there are several groups depending on the reverse recovery characteristic (reverse recovery time trr):

- Standard rectifiers with a trr $>$ 500 ns
- Fast rectifiers with a 100 ns $<$ trr $<$ 500 ns
- Ultrafast rectifiers with a trr $<$ 100 ns
- Schottky rectifiers with majority carrier effect

Excluding Schottky rectifiers, all these are of p-n junction technology with different processes to optimize their characteristics. Schottky rectifiers have an interesting characteristic, they present excellent switching characteristics compared to even the fastest p-n junction diode.

4.3.2 Schottky Rectifiers

The primary assets of Schottky devices are switching speeds, approaching zero-time, and very low forward voltage drop (V_F). This combination makes Schottky barrier rectifiers ideal for the output stages of switching power supplies. On the negative side, Schottky devices are also known for limited high-temperature operation, high leakage and limited voltage range (Break down Voltage), V_{BR}. Though these limitations exist, they are quantifiable and controllable.

4.3.3 In circuit behavior

T_{on} phase

During the t_{on} phase there is no forward current flowing through the rectifier, it is reverse-biased. The parameters involved in the steady state of this phase which I take into account for selecting a diode are the following:

- V_R - Reverse voltage
  - The boost converters maximum output voltage is the reverse voltage which the diode will experiment during this phase.
- V_{RRM} - Repetitive peak reverse voltage, including all repeated reverse transient voltages
  - The repetition rate at which it is exposed to this voltage is defined by the switching frequency, as it is exposed to this voltage difference once every phase during a maximum period of the t_{on} phase.
- V_{BR} - Reverse breakdown voltage
  - Satisfying the reverse voltage this specification is satisfied as well.
- I_R - Reverse (leakage) current, at a specified reverse voltage VR and temperature TJ.
  - The reverse leakage current will decrease the output voltage as it is another load for the output. The levels are negligible when compared to other loses.

$$V_{BR} \geq V_{RRM} \geq V_R \geq 2 \cdot 12V = 24V$$

Transition $t_{off} \rightarrow t_{on}$

During the transition from the t_{off} phase to the t_{on} phase, the losses are directly related to the time taken to go from non-conduction mode to conduction mode, this is known as the reverse recovery time (trr). In a p-n diode the reverse recovery time can be in the order of hundreds of nanoseconds and less than 100 ns for ultra fast diodes, Schottky diodes do not have a recovery time, as there is nothing to recover from. The switching time is $\approx$ 100 ps for the small signal diodes, and up to tens of nanoseconds for special high-capacity power diodes. With Schottky diodes switching essentially instantly, the component of choice.

T_{off} phase

During the t_{off} phase the energy accumulated in the inductor during the complementary phase (t_{on}) will need to pass through the rectifier. The quantity of concern is the peak current and the amount of power dissipated by the diode, this is where the following parameters come into consideration.

- I_{FSM} - Peak forward surge current.
  - The peak current in our application for the proposed inductance of 680nH was 39.2A, calculated in section 4.1, should be our reference which should be satisfied.
- $I_{F(AV)}$ - Average forward output current.
  - $I_{avg} = I_{peak} \times \frac{t_{off}}{T}$, where the worst case scenario presents itself at the lowest input voltage. $I = \frac{P}{V} = \frac{4W}{0.7V} = 5.7A$.
- V_F - Forward voltage drop, at a specified forward current I_F and junction temperature T_J.
  - The aim is to get the lowest possible voltage drop as this quantity will determine how much power is being dissipated by the diode. $P_{avg} = I_{avg} \times V_F$

Component Selection

Farnell Code	Part Number	V_{RRM}	Max V_f	I_{FSM}	$I_{F_{avg}}$
1570041	SS10P3CL-E3/86A	30V	420mV	200A	2×5A

4.4 Switching element

The semiconductor which I have chosen to act as switching element is an N-type Power Mosfet.

4.4.1 Mosfet Parameters

Parameters which classify a mosfet for a particular application include the following:

- On-state resistance
- Breakdown voltage
- Capacitances
- Gate oxide breakdown
- Maximum drain to source voltage
- Maximum drain current
- Maximum temperature

4.4.2 Maximum drain current

The mosfet is working during the first phase, the t_{on} phase, of the cycle. It "charges" the inductor to a peak current I_{peak} which depends on the input voltage and the duration of the phase.

DCM

With the topology setup to work in DCM, theoretically, our peak current for the proposed inductance of 680nH was 39.2A, calculated in section 4.1.

This current is very high but it has also been calculated in an ideal case and in any case it is only momentarily as the current increases from 0 to this peak value in 6.7 μseconds. This leads me to investigate actually the maximum d_i/d_t of the inductance which I have chosen as this will limit the real maximum current which the inductor can reach in a given time period.

The real circuit input at this moment is the input voltage source which consists of a charged capacitor, with its equivalent series resistance (ESR), on the sourcing side of the inductance which has its inherit dc resistance (specified in the datasheet) and the R_{dson} resistance of the chosen mosfet on the tailing end. We see that a simplified real input circuit presents the following characteristics:

The input capacitor ESR is approximately 10mΩ and the DCR of the inductance is 1.6mΩ. The mosfets which I am filtering for selection have ranging on state resistances from 3mΩ to 30mΩ.

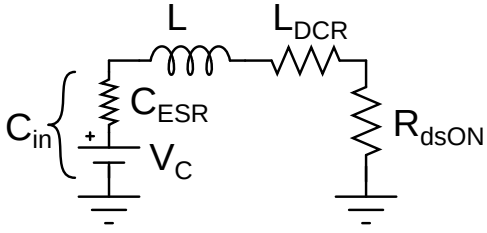


Figure 4.1: Equivalent t_{on} phase circuit

The current characteristics of a series L-R circuit can be calculated as:

$$I(t) = \frac{V}{R}(1 - e^{-t/\tau}) \quad , \quad \tau = \frac{L}{R}$$

Since the mosfet has not been chosen yet, as a guide I have plotted several R_{dsON} cases maintaining the following parameters:

t_{on}	V_{in}	L
6.7 μs	4 V	680 nH

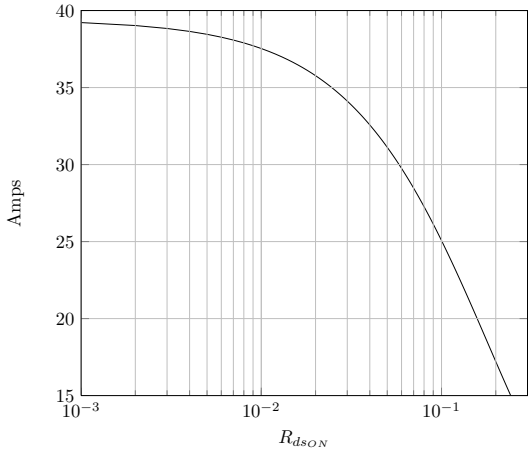


Figure 4.2: Peak current in Mosfet vs. R_{on}

As the plot shows, the maximum current reached does not vary much within the range of on-resistances of mosfets proposed.

DCM Maximum drain current $\geq$ 35 Amps.

CCM

With the topology setup to work in CCM, theoretically, our peak current is defined by:

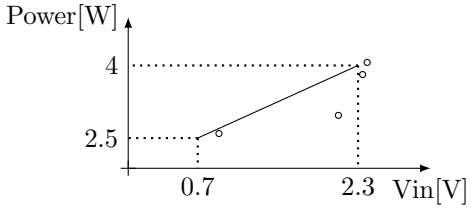
$$I_{peak} = I(0) + \frac{V_{in} t_{on}}{L} \qquad t_{on} \leq \frac{1}{f_{SW}} \cdot \frac{V_{out} - V_{in}}{V_{out}}$$

Here we can see a difference in the peak current due to a "residual" current which remains is the inductor throughout both phases. To minimize conduction losses in the mosfet it is recommended to maintain the ripple current ΔI_L below 30% of the residual current. As the circuit is working in CCM the relation between the output and inductor current is as follows:

$$I_{L_{avg}} = \frac{I_o}{1-D} \qquad I_o = \frac{P}{V_o} \qquad V_o = \frac{V_i}{1-D}$$

$$I_{L_{avg}} = \frac{\frac{P}{\frac{V_i}{1-D}}}{1-D} = \frac{P}{V_i} \qquad I_{max} \rightarrow V_{min}$$

$$= 2.5/0.7 = 3.57 Amps$$



To calculate the maximum ripple current I will set the input voltage to its maximum and the duty cycle as well. Given that for CCM I have chosen a 100 μH sized inductor our ripple current will be always below 400mA.

CCM Maximum drain current $\geq$ 4 Amps.

4.4.3 On-state resistance

To minimize losses it is desirable to have the lowest On-state resistance possible but this is normally proportional to the maximum drain current that the mosfet can withstand. Therefore this is not going to be a search criteria but a parameter to take into account once a mosfet has been chosen.

Breakdown voltage/on-state resistance trade-off

The on-state resistance is a sum of several resistances where one of them, R_n, is the resistance of the epitaxial layer. The role of this layer is to sustain the blocking voltage, R_n is directly related to the voltage rating of the device. A high voltage MOSFET requires a thick, low-doped layer, whereas a low-voltage transistor only requires a thin layer with a higher doping level. As a result, R_n is the main factor responsible for the resistance of high-voltage MOSFETs.

4.4.4 Breakdown voltage

The theoretical maximum voltage the mosfet is exposed to is $V_{out_{max}} + V_{D_{max}}$. There is an overshoot voltage which occurs when the inductor charging cycle ends and the inductor current is released to the load. The overshoot voltage is a function of the inductor, output capacitor, Peak Inductor Current, output current, input voltage, output voltage, and an estimate of the voltage drop across the diode ($\approx$ 0.5v). The overshoot voltage is improved by increasing the output capacitance but degrades slightly with increasing input voltage.

To calculate a possible overshoot voltage the diode is an important element which needs to be brought into conduction as soon as possible.

Calculations for the overshoot voltage and what I can do to decrease this peak due to parasitic capacitances and inductances are discussed in section 4.5. For the meantime I will scale the theoretical maximum by 2 and round up to have a safety margin.

$$\text{Breakdown voltage} \geq 30 \text{ V}$$

4.4.5 Power Losses

The power losses associated with the mosfet are summarized in table 4.6:

Losses	Description	Losses
Conduction	These losses are associated with the mosfet ON time. I_{rms} depends on the duty cycle and the load current.	$P_{Cond} = I_{rms}^2 \times R_{ds_{ON}}$
Gate Drive	These losses are associated with charging and discharging the gate of the mosfet every cycle. Q_G is the total gate charge.	$P_{IN} = V_G \times Q_G \times f_{sw}$
Switching	These are the losses during the drain voltage and drain current transitions for every cycle. Losses occur during the transition between the two phases, $t_{on} \leftrightarrow t_{off}$	$P_{sw} = V_{in} \times I_L \frac{Q_{sw}}{I_G} \times f_{sw}$
Output	These losses are associated with the Q_{OSS} of the device	$P_{out} = \frac{Q_{OSS}}{2} \times V_{in} \times f_{sw}$

Table 4.6: MOSFET power losses summary

4.4.6 Temperature influence

Power derating

On average the application will be attempting to be as efficient as possible. This implies that power dissipation will be reduced to a minimum. The devices which are rated at the high currents which I will be working at are rated to dissipate more than 50Watts. The design will be dissipating less than 250mW. There fore the power derating is not of our concern.

Threshold voltage

With lower temperature the gate to source voltage applied permits less current to flow through. Threshold voltage is inversely proportional to temperature. I have observed from several datasheets $\approx$15% increase at -40°C compared to the minimum threshold value at 25°C. This requires me to search for a $V_{gs_{th}} \leq 2.5V$@-40°C this translates to a $V_{gs_{th}} \leq 2.15V$@-40°C.

4.4.7 Component selection

Going through the main distributor, Farnell, I have the following requirements to fulfill:

Maximum drain current	$\geq$ 35 Amps
Breakdown voltage	$\geq$ 30 V
Threshold Voltage	$\leq$ 3 V

The parameters I_d@3V_{gs} and I_d@2.5V_{gs} are drain current at a junction temperature of 25°C and with a V_{ds} of 1V. The equivalent on-state resistance can be calculated using Ohms-Law. The parameter Q_g is the total gate charge measured with a V_{gs} of 4.5V

Part Name	Farnell Code	I_d@3V_{gs}	I_d@2.5V_{gs}	Q_g	$I_{ds_{max}}$	$V_{ds_{max}}$
PSMN2R0-30YL	1699703	93A	20A	30nC	100A	30V
PSMN2R5-30YL	1699704	83A	18A	27nC	100A	30V
PSMN3R0-30YL	1699705	75A	16A	21nC	100A	30V
PSMN3R5-30YL	1699706	74A	18A	19nC	100A	30V
PSMN4R0-30YL	1699707	67A	18.5A	17.6nC	76A	30V
PSMN5R0-30YL	1699708	45A	12A	14.1nC	64A	30V
PSMN6R0-30YL	1699709	22A	3A	11nC	56A	30V
PSMN7R0-30YL	1699710	32A	7A	10nC	53A	30V
PSMN9R0-30YL	1699711	30A	7A	8.7nC	43A	30V
PH7030L	1081444	24A	7.5A	12nC	43A	30V
PH3830L	1081443	36A	6.5A	33nC	62A	30V
SIE848DF-T1-GE3	1779243	62A	-	43nC	60A	30V
IRLR8503PbF	8651302	30A	3A	15nC	32A	30V

Given the wide variety that all the PSMNxxx parts give me and that they are all in the same package format I am going to use that package format as a footprint and start off with the PSMN3R5-30YL with farnell code 1699706.

Selected MOSFET: **PSMN3R5-30YL** fc:1699706

4.5 Snubber Investigation

4.5.1 Introduction

The main switching element has a current and voltage limit. Exceeding the current limit will provoke overheating of the device and it will eventually fail. According to simulations and calculations the current limits will not be exceeded but the voltage "ringing", if there is any, may come close to datasheet specified absolute maximums. Therefore to "clamp" the voltage between the drain-source I will calculate a simple snubber circuit.

4.5.2 Snubber explanation

A basic classical boost converter is shown in figure 4.3. I have modeled the load as a resistor.

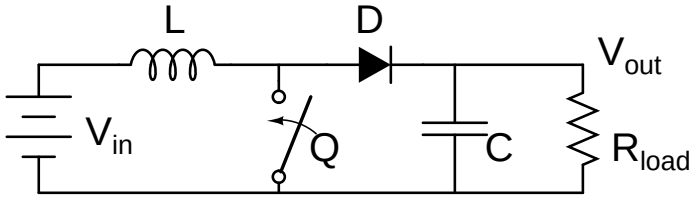


Figure 4.3: Boost converter component layout

For snubber design we are concerned with circuit behavior during the switch transition time which is much shorter than the switching period. This allows us to simplify the analysis. In normal operation the output voltage is DC with very little ripple. This means that we can replace the load and filter capacitor with a battery since the output voltage changes very little during switch transitions. The current in the inductor will also change very little during a transition, by definition, and we can replace the inductor with a current source. The simplified circuit is presented in figure 4.4.The voltage (V_Q) and current (I) waveforms are given in figure 4.5.

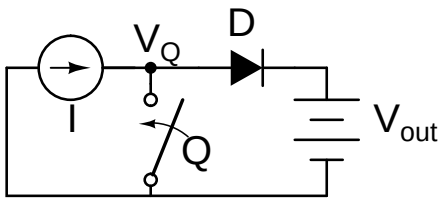


Figure 4.4: Simplified circuit with loaded inductor

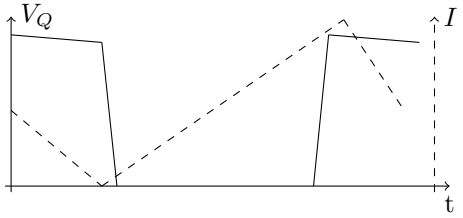


Figure 4.5: Waveforms durring turn on/off transitions

At the beginning of the switching cycle the switch is open and all of the current (I) will be flowing through the diode into the battery. As the switch turns on, the current will gradually shift from the diode to the switch. However, as long as there is current in the diode, the switch voltage will remain at V_{out}. Once all of the current has been transferred to the switch, the switch voltage can begin to fall. At turn-off the situation is reversed. As the switch turns off, the voltage across it will rise. The current in the switch will however, not begin to fall until the switch voltage reaches $V_{out} + V_{D_f}$ because the diode will be reverse biased until that point. Once the diode begins to conduct the current in the switch can fall.

This type of switching, commonly referred to as "hard switching", exposes the switch to high stress because the maximum voltage and maximum current must be supported simultaneously. This also leads to high switching loss. In practical circuits the switch stress will be even higher due to the unavoidable presence of parasitic inductance (L_p) and capacitance (C_s) as shown in figure 4.6.

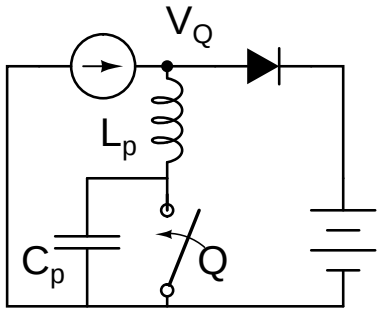


Figure 4.6: Switch parasitic components

C_p includes the junction capacitance of the switch and stray capacitance due to circuit layout and mounting. L_p is due to the finite size of the circuit layout and lead inductance. L_p can be minimized with good layout practice but there maybe some residual inductance which may cause a ringing voltage spike at turn-off. The most common reasons for using a snubber are to limit the peak voltage across the switch and to reduce the switching.

4.5.3 RC snubber design

An RC snubber, placed across the switch as shown in figure xx, can be used to reduce the peak-voltage at turn-off and to damp the ringing. In most cases a very simple design technique can be used to determine suitable values for the snubber components (R_s and C_s). In those cases where a more optimum design is needed, a somewhat more complex procedure is used.

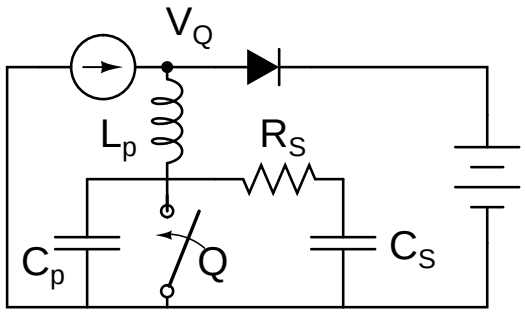


Figure 4.7: Equivalent circuit with parasitic components and snubber

Design Procedure

To achieve significant damping $C_s > C_p$. A good first choice is to make C_s equal to twice the sum of the output capacitance of the switch and the estimated mounting capacitance. R_s is selected so that $R_s = V_o/I_o$. This means that the initial voltage step due to the current flowing in R_s is no greater than the clamped output voltage. The peak power dissipated in R_s can be estimated from peak energy stored in C_s:

$$E_{peak} = \frac{C_s V_{out}^2}{2}$$

This is the amount of energy dissipated in R_s when C_s is charged and discharged so that the average power dissipation at a given switching frequency (f_s) is:

$$P_{avg} = E_{peak} \cdot f_{sw}$$

Depending on the amount of ringing the actual power dissipation will be slightly higher than this.

Applied to circuit

The Mosfet I have selected for this application has the part number: PSMN3R5-30YL. At 9 Volts the mosfet presents a bit over 600pF for C_{oss} and at 12 Volts 532pF, I will suppose a mounting capacitance of $\approx 50pF$. Doubling this capacitance for C_S is $\approx 1.2nF$.

$$\begin{aligned} R_s =& \frac{V_o}{I_o} \qquad P = I \cdot V \\ =& \frac{V_o^2}{P_{max}} = \frac{12^2}{4} = 16\Omega \end{aligned}$$

The average power dissipated in the resistance:

$$\begin{aligned} E_{peak} =& \frac{1.2nF \cdot 12^2}{2} = 86.4nJ \\ P_{avg} =& 86.4nJ \cdot 100kHz = 8.64mW \end{aligned}$$

As low power is going to be dissipated in the resistance, I will use average SMD sized 0805 resistances and capacitors to implement this snubber.

Chapter 5

Maximum Power Point Trackers

A maximum power point tracker (MPPT) is generally known as a power electronic DC-DC converter inserted between the Photo-Voltaic (PV) module and its load to achieve optimum matching. More precisely the MPPT is an intelligent algorithm that ensures the PV module always operates at its maximum power point as the temperature, insolation and load vary. A number of tracking algorithms have been proven and used and a number of DC-DC converter topologies are possible.

5.1 The Objective

Figure 5.1 shows the characteristic power curve for a photo voltaic cell.

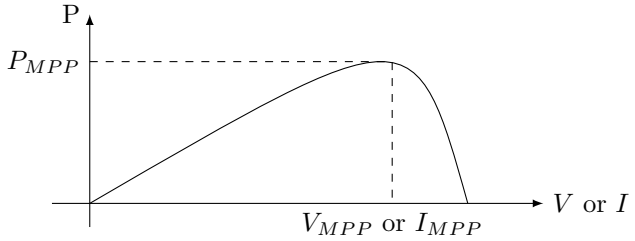


Figure 5.1: Characteristic PV power curve

The problem considered by MPPT techniques is to automatically find the voltage V_{MPP} or current I_{MPP} at which a PV-cell should operate to obtain the maximum power output P_{MPP} under a given temperature and irradiance. Under partial shading conditions, in some cases it is possible to have multiple local maxima, but overall there is still only one true MPP. Most techniques respond to changes in both irradiance and temperature, but some are specifically more useful if temperature is approximately constant. Most techniques would automatically respond to changes due to aging, though some are open-loop and would require periodic fine-tuning.

5.2 Hill Climbing and P&O

Hill climbing involves a perturbation in the duty ratio of the power converter, and P&O, perturbation and observation, a perturbation in the operating voltage of the PV cell. In the case of a PV cell connected to a power converter, perturbing the duty ratio of power converter perturbs the PV current and consequently perturbs the PV voltage. Hill climbing and P&O methods are different ways to envision the same fundamental method.

5.2.1 Description

From figure 5.1, it can be seen that incrementing/decrementing the voltage increases/decreases the power when operating on the left of the Maximum Power Point (MPP) and decreases/increases the power when on the right of the MPP. Therefore, if there is an increase in power, the subsequent perturbation should be kept the same to reach the MPP and if there is a decrease in power, the perturbation should be reversed. This algorithm is summarized in table 5.1.

Perturbation	Change in Power	Subsequent Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

Table 5.1: Hill Climbing and P&O Algorithm

The process is repeated periodically until the MPP is reached. The system then oscillates about the MPP. The oscillation can be minimized by reducing the perturbation step size. However, a smaller perturbation size slows down the MPPT. A solution to this conflicting situation is to have a variable perturbation size that gets smaller towards the MPP as is typical in other convergence methods.

Inputs

Two sensors are usually required to measure the PV voltage and current from which power is computed, but depending on the power converter topology, only a voltage sensor might be needed.

5.2.2 Temporary Divergence

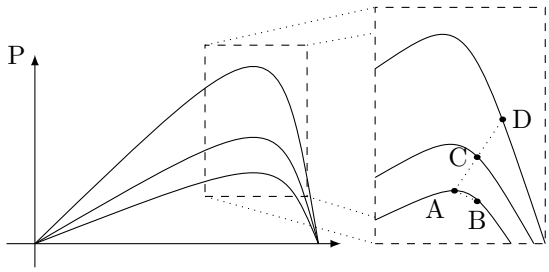


Figure 5.2: Divergence of hill climbing/P&O algorithm

Hill climbing and P&O methods can fail under rapidly changing atmospheric conditions as illustrated in figure 5.2. Starting from an operating point A, if atmospheric conditions stay approximately constant, a perturbation ΔV in the PV voltage V will bring the operating point to B and the perturbation will be reversed due to a decrease in power. However, if the irradiance increases and shifts the power curve from the lower to the higher within one perturbation update period, the operating point will move from A to C. This represents an increase in power and the perturbation is kept the same. Consequently, the operating point diverges from the MPP and will keep diverging if the irradiance steadily increases.

To ensure that the MPP is tracked even under sudden changes in irradiance, a three-point weight comparison P&O method that compares the actual power point to two preceding ones before a decision is made about the perturbation sign can be used or simply the sampling rate can be increased.

5.3 Incremental Conductance

The incremental conductance (IncCond) method is based on the fact that the slope of the PV cell power curve, figure 5.1 is zero at the MPP, positive on the left of the MPP, and negative on the right, as given by table 5.2.

$dP/dV = 0,$	at MPP
$dP/dV > 0,$	left of MPP
$dP/dV < 0,$	right of MPP

Table 5.2: MPP Slope Characteristics

Since,

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \approx I + V\frac{\Delta I}{\Delta V} \tag{5.1}$$

Table 5.2 can be reformulated to table 5.3:

$\Delta I/\Delta V = -I/V,$	at MPP
$\Delta I/\Delta V > -I/V,$	left of MPP
$\Delta I/\Delta V < -I/V,$	right of MPP

Table 5.3: MPP Slope Characteristics as a function of current and voltage

The MPP can therefore be tracked by comparing the instantaneous conductance (I/V) to the incremental conductance ($\Delta I/\Delta V$).

5.3.1 Description

Vref is the reference voltage at which the PV cell is forced to operate. At the MPP, V_{ref} equals to V_{MPP}. Once the MPP is reached, the operation of the PV cell is maintained at this point unless a change in ΔI occurs, indicating a change in atmospheric conditions and therefore, the MPP. The algorithm decrements or increments V_{ref} to track the new MPP.

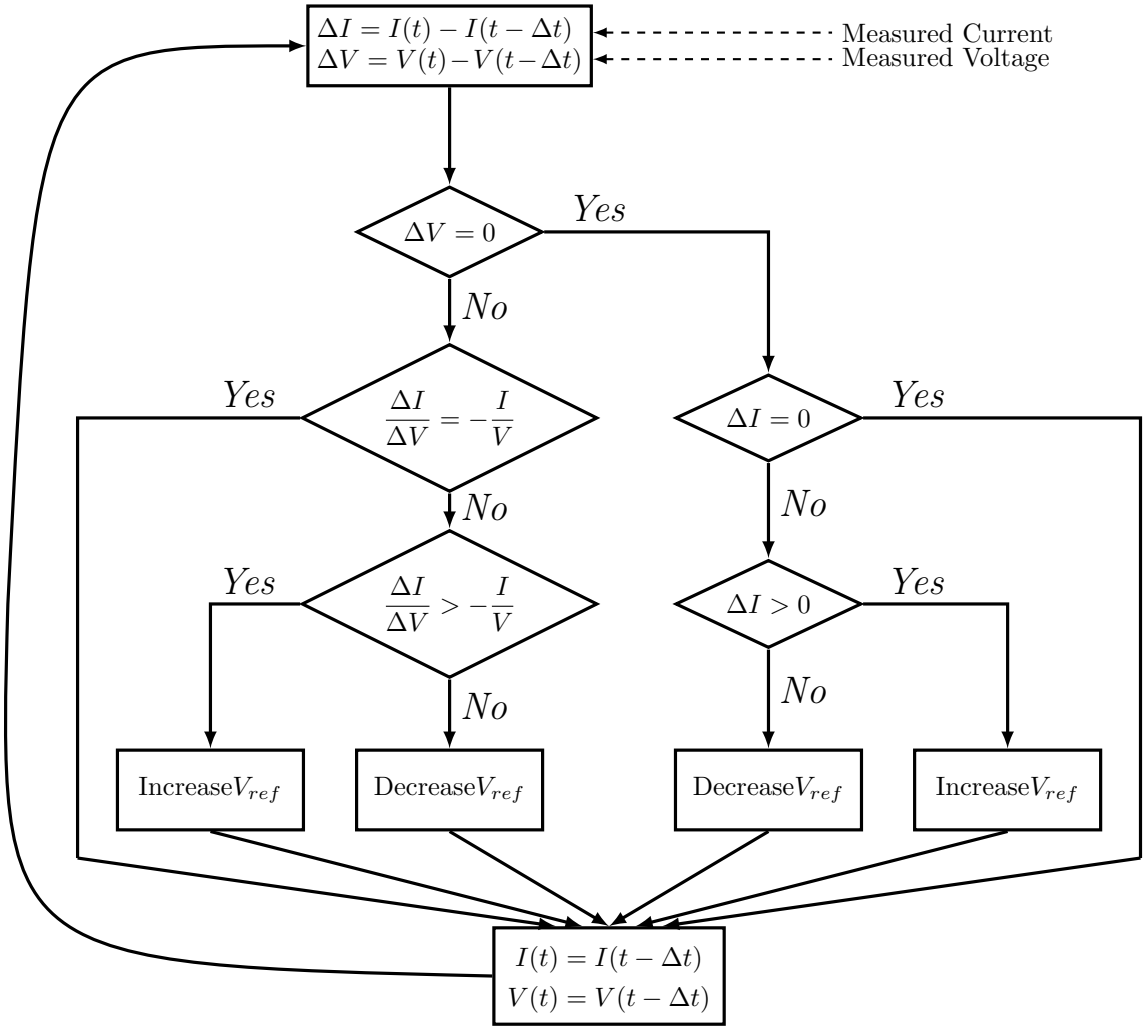


Figure 5.3: Incremental Conductance flow diagram

As can be seen from figure 5.3, the increment size determines how fast the MPP is tracked. Fast tracking can be achieved with bigger increments but the system might not operate exactly at the MPP and oscillate around it instead, there is a trade off. An effective way of performing the IncCond technique is to use the instantaneous conductance and the incremental conductance to generate an error signal:

$$e = \frac{I}{V} + \frac{dI}{dV} \tag{5.2}$$

From table 5.2 we can deduce that the error, e, goes to zero at MPP. A simple proportional integral control can then be used to drive e to zero.

Inputs

Measurements of the instantaneous PV voltage and current require two sensors. IncCond method lends itself well to digital controllers, which can easily keep track of previous values of voltage and current to make all the required decisions. An analog implementation is not as simple.

5.4 Fractional Open-Circuit Voltage

The near linear relationship between V_{MPP} and V_{OC} of the PV cells, under varying irradiance and temperature levels, has given rise to the fractional V_{OC} method.

$$V_{MPP} \approx k \cdot V_{OC} \tag{5.3}$$

k is a constant of proportionality. Since k is dependent on the characteristics of the PV cell being used, it usually has to be computed beforehand by empirically determining V_{MPP} and V_{OC} for the specific cell at different irradiance and temperature levels. Typical values for k are between 0.71 and 0.78.

Once k is known, V_{MPP} can be computed using equation 5.3 with V_{OC} being measured periodically by momentarily shutting down the power converter. As can clearly be imagined already their are some inherit disadvantages, the most obvious being temporary loss of power. To prevent this, one can use "guidance" cells from which V_{OC} can be obtained. These guidance cells must be carefully chosen to closely represent the characteristics of the PV cell. Once V_{MPP} has been approximated, a closed-loop control on the power converter can be used to asymptotically reach this desired voltage.

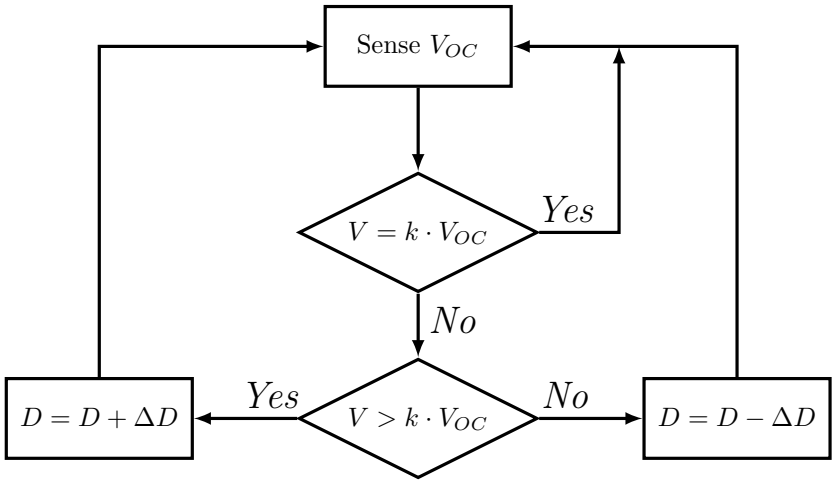


Figure 5.4: Fractional Open circuit Voltage flow diagram

Since equation 5.3 is only an approximation, the PV cell technically never operates at the MPP. Depending on the application of the PV system, this can sometimes be adequate. Even if fractional V_{OC} is not a true MPPT technique, it is very easy and cheap to implement as it does not necessarily require DSP or micro controller control. However, in the presence of partial shading (which causes multiple local maxima) of the PV cells, the proportionality constant, k, is no more valid and will need to be updated by sweeping the PV cells power values. This obviously adds to the implementation complexity and involves more power loss.

5.5 Fractional Short-Circuit Current

Fractional I_{SC} results from the fact that, under varying atmospheric conditions, I_{MPP} is approximately linearly related to the short circuit current, I_{SC}, of the PV cell.

$$I_{MPP} \approx k \cdot I_{SC} \tag{5.4}$$

k is a proportionality constant. Just like in the fractional V_{OC} technique, k has to be determined according to the PV-cell in use. The constant is generally found to be between 0.78 and 0.92. Substituting fractional voltage for current in the flow diagram in figure 5.4 depicts the process to follow.

Measuring I_{SC} during operation is requires an additional switch to be added to the power converter to periodically short the PV array so that I_{SC} can be determined using a current sensor. This increases the number of components and cost. In a boost converter topology the input is shorted during one part of the cycle and this then allows for double functionality of an already existing component.

While measuring the short circuit current, output power is reduced. Inherent to the approximation is the fact that the MPP is never perfectly matched. To guarantee proper MPPT in the presence of multiple local maxima, periodic sweeps of the PV cell from open circuit to short circuit can be introduced to update k.

5.6 Fuzzy Logic Control

Fuzzy logic controllers have the advantages of working with imprecise inputs, not needing an accurate mathematical model, and handling well nonlinearities.

Fuzzy logic control generally consists of three stages:

- Fuzzification: Numerical input variables are converted into linguistic variables based on a membership function.
- Rule base table lookup: Where the decision is taken, fuzzy output defined.
- Defuzzification: The fuzzy logic controller output is converted from a linguistic variable to a numerical variable.

The fuzzification represented in figure 5.5 has five fuzzy levels listed in table 5.4, a and b are based on the range of values of the numerical variable. The membership function is sometimes made less symmetric to give more importance to specific fuzzy levels.

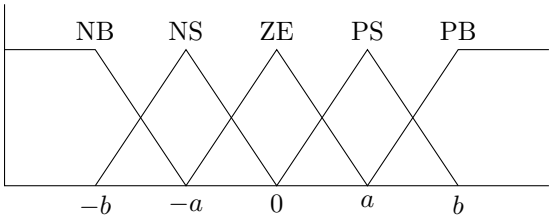


Figure 5.5: Membership function of fuzzy controller

NB:	negative big
NS:	negative small
ZE:	zero
PS:	positive small
PB:	positive big

Table 5.4: Fuzzification levels

The inputs to a MPPT fuzzy logic controller are usually an error ϵ and a change in error $\Delta\epsilon$. The user has the flexibility of choosing how to compute ϵ and $\Delta\epsilon$. Since $\frac{dP}{dV} = 0$ at the MPP we can use the approximations:

$$\epsilon(n) = \frac{P(n) - P(n-1)}{V(n) - V(n-1)} \tag{5.5}$$

$$\Delta\epsilon(n) = \epsilon(n) - \epsilon(n-1) \tag{5.6}$$

Equation 5.2 also is a valid definition for the error. Once these have been calculated and converted into linguistic variables, the fuzzy logic controller output, which is typically a change in duty ratio ΔD, can be looked up in a rule base table such as table 5.5.

ϵ \ $\Delta\epsilon$	NB	NS	ZE	PS	PB
NB	ZE	ZE	NB	NB	NB
NS	ZE	ZE	NS	NS	NS
ZE	NS	ZE	ZE	ZE	PS
PS	PS	PS	PS	ZE	ZE
PB	PB	PB	PB	ZE	ZE

Table 5.5: Fuzzy Rule base table

The linguistic variables assigned to ΔD for the different combinations of ϵ and $\Delta\epsilon$ are based on the power converter being used and also on the knowledge of the user. If, for example, the operating point is far to the left of the MPP, ϵ is PB and $\Delta\epsilon$ is ZE, then we want to largely increase the duty ratio, ΔD should be PB to reach the MPP. The defuzzification stage will translate PB to an analog signal that will control the power converter to the MPP.

MPPT fuzzy logic controllers have been shown to perform well under varying atmospheric conditions. Their effectiveness greatly depends on the knowledge of the user or control engineer in choosing the right error computation and coming up with the rule base table. Adaptive fuzzy logic controls update the rule base table according to measured parameters and therefore depend less on the initial knowledge.

5.7 Neural Network

Along with fuzzy logic for MPPT algorithms came neural networks. These are more specific and therefore less flexible to design alterations.

Neural networks commonly have three layers: input, hidden, and output layers. The number of nodes in each layer vary and are user-dependent. The input variables can be PV parameters like V_{OC} and I_{SC}, atmospheric data like irradiance and temperature, or any combination of these.

The output is usually one or several reference signals like a duty cycle signal used to drive the power converter to operate at or close to the MPP. How close the operating point gets to the MPP depends on the algorithms used by the hidden layer and how well the neural network has been trained. The links between the nodes are all weighted. To accurately identify the MPP, the weights have to be carefully determined through a training process, whereby the PV cell is tested over months or years and the patterns between the inputs and outputs of the neural network are recorded.

Since most PV cells have different characteristics, a neural network has to be specifically trained for the PV cell with which it will be used. The characteristics of a PV array also change with time, implying that the neural network has to be periodically trained to guarantee accurate MPPT.

5.8 Ripple correlation control

When a PV cell is connected to a power converter, the switching action of the power converter imposes voltage and current ripple on the cell. As a consequence, the PV cell power is also subject to ripple. Ripple correlation control (RCC) makes use of ripple to perform MPPT. RCC correlates the time derivative of the time-varying PV power p' with the time derivative of the time-varying PV current i' or voltage v' to drive the power gradient to zero, thus reaching the MPP.

If the voltage or current are increasing ($v' > 0$ or $i' > 0$) and the power is increasing ($p' > 0$), then the operating point is below(to the left) the MPP, ($V < V_{MPP}$ or $I < I_{MPP}$). If instead, given the same voltage current conditions, the power is decreasing ($p' < 0$), then the operating point is above (to the right) the MPP. The first case is plotted with hollow dots and the second with filled dots in figure 5.6.

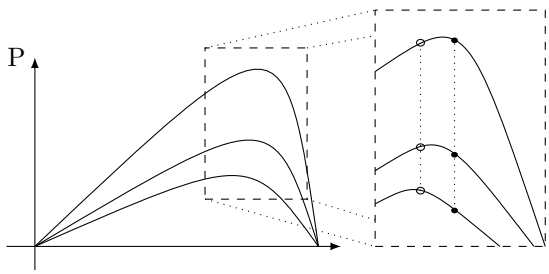


Figure 5.6: MPPT loss due to no update

Combining these observations, we see that $p'v'$ or $p'i'$ are positive to the left of the MPP, negative to the right of the MPP and zero at the MPP.

When the power converter is a boost converter, increasing the duty ratio increases the inductor current and therefore also the PV current. Therefore, the duty ratio control input is:

$$d(t) = -k \int p'v'dt \tag{5.7}$$

$$d(t) = k \int p'i'dt \tag{5.8}$$

where k is a positive constant. Controlling the duty ratio in this way assures that the MPP will be continuously tracked.

The derivatives are usually undesirable as they slow down the algorithm and are prone to error from inaccurate measurements. AC-coupled measurements of the PV current and voltage can be used instead since they contain the necessary phase information. The derivatives can also be approximated by high-pass filters with cut-off frequency higher than the ripple frequency. A different and easy way of obtaining the current derivative is to sense the inductor voltage which is proportional to the current derivative. The nonidealities in the inductor such as core loss and series resistance have a small effect since the time constant of the inductor is much larger than the switching period in a practical converter.

Simple and inexpensive analog circuits can be used to implement RCC. The time taken to converge to the MPP is limited by the switching frequency of the power converter and the gain of the RCC circuit. This method does not require any prior information about the PV array characteristics, making its adaptation to different layouts simple.

5.9 Current Sweep

The current sweep method uses a sweep waveform for the PV current such that the current-voltage (I-V) characteristic of the PV cell is obtained and updated at fixed time intervals. The V_{MPP} can then be computed from the characteristic curve at the same intervals. The function chosen for the sweep waveform is directly proportional to its derivative as in

$$f(t) = k\frac{df(t)}{dt} \tag{5.9}$$

where k is a proportionality constant. The PV array power is therefore given by

$$p(t) = v(t) \cdot i(t) = v(t) \cdot f(t) \tag{5.10}$$

At the Maximum power point

$$\frac{dp(t)}{dt} = v(t)\frac{df(t)}{dt} + f(t)\frac{dv(t)}{dt} = 0 \tag{5.11}$$

$$= \left[v(t) + k\frac{dv(t)}{dt}\right]\frac{df(t)}{dt} = 0 \tag{5.12}$$

The differential equation has the following solution

$$f(t) = C \cdot e^{\frac{t}{k}} \tag{5.13}$$

C is chosen to be equal to the maximum PV current, I_{max} and k to be negative, resulting in a decreasing exponential function with time constant $\tau = -k$, substituting in equation 5.13:

$$f(t) = I_{max}e^{\frac{t}{\tau}} \tag{5.14}$$

The current, $f(t)$, can be obtained by using some current discharging through a capacitor. Since the derivative of equation 5.14 is nonzero, equation 5.12 can be divided by $\frac{df(t)}{dt}$ and with $f(t) = i(t)$, equation 5.12 simplifies to

$$\frac{dp(t)}{di(t)} = v(t) + k\frac{dv(t)}{dt} \tag{5.15}$$

Once V_{MPP} is computed after the current sweep, equation 5.15 can be used to double check whether the MPP has been reached.

This method requires additional components and some loss of the available power.

5.10 Load Current or Load Voltage Maximization

The purpose of MPPT techniques is to maximize the power coming out of a PV cell. When the PV cell is connected to a power converter, maximizing the PV power also maximizes the output power at the load of the converter. Conversely, maximizing the output power of the converter should maximize the PV power, assuming a lossless converter.

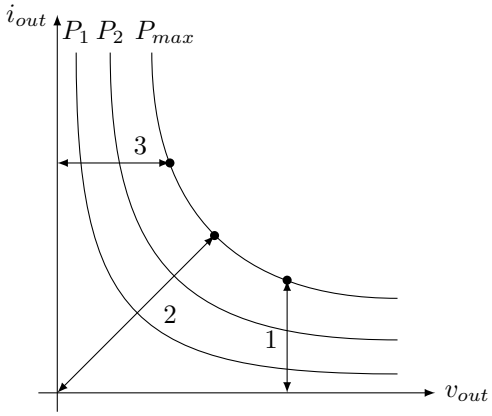


Figure 5.7: Different load types, 1: voltage source, 2: resistive, 3: current source

Most loads can be of voltage-source type, current-source type, resistive type, or a combination of these, as shown in figure 5.7. From this figure, it is clear that for a voltage-source type load, the load current i_{out} should be maximized to reach the maximum output power P_{max}. For a current-source type load, the load voltage v_{out} should be maximized. For the other load types, either i_{out} or v_{out} can be used. This is also true for nonlinear load types as long as they do not exhibit negative impedance characteristics. Therefore, for almost all loads of interest, it is adequate to maximize either the load current or the load voltage to maximize the load power. Only one sensor is needed.

In most PV systems, a battery is used as the main load or as a backup. Since a battery can be thought of as a voltage-source type load, the load current can be used as the control variable. Positive feedback can be used to control the power converter such that the load current is maximized and the PV cell operates close to the MPP. Operation exactly at the MPP is almost never achieved because this MPPT method is based on the assumption that the power converter is lossless.

5.11 $\frac{dP}{dV}$ or $\frac{dP}{dI}$ Feedback Control

With DSP and micro controllers being able to handle complex computations, an obvious way of performing MPPT is to compute the slope ($\frac{dP}{dV}$ or $\frac{dP}{dI}$) of the PV power curve and feed it back to the power converter with some control to drive it to zero. The way the slope is computed differs from paper to paper.

In one implementation, $\frac{dP}{dV}$ is computed and its sign is stored for the past few cycles. Based on these signs, the duty ratio of the power converter is either incremented or decremented to reach the MPP. A dynamic step size is used to improve the transient response of the system.

This method is prone to error and limited by the accuracy of the sensing methods or equipment.

5.12 Other Techniques

- A linear current control based on a linear relationship between I_{MPP} and the irradiance level.
- A state-based MPPT where the system is represented by a state space model and a nonlinear time varying dynamic feedback controller is to track the MPP.

- The Best Fixed Voltage (BFV): based on statistical data and is dependent on the geographical location of the tracker.
- A Linear reoriented coordinates method (LRCM): requires to measure the V_{OC} and I_{SC} amongst other parameters as it iteratively calculates a model representing the PV cell and defines the operating point.

5.13 Comparison

With so many MPPT techniques available it may be difficult to choose which one suits us best. The main aspects of the MPPT techniques are expressed in table 5.6.

MPPT Method	PV cell dependent	True MPPT	Analog / Digital	Periodic tunning	Convergence	Complexity	Parameters
Hill Climbing / P&O	No	Yes	A/D	No	Varies	Low	Voltage, Current
IncCond	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	A/D	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	A/D	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analog	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
Load I or V Mazimization	No	No	Analog	No	Fast	Low	Voltage, Current
$\frac{dP}{dV}$ or $\frac{dP}{dI}$ Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

Table 5.6: Summary of MPPT Algorithm characteristics

Chapter 6

Proposed Design

The objective of this thesis is to propose a design to evaluate the feasability of elevating the input voltage following the maximum power point given by some solar cells. In sections 1.1, 1.2 and 1.3 we introduced several topologies to be able to step up the voltage. To analyze the physical limits of the classical boost converter, introduced in section 1.1, I have decided to design the application around this converter operating in both continuous conduction mode and discontinuous conduction mode. The equations used to design the stage are derived in chapter 2. The specifications to which we will adhere are determined in chapter 3 and the calculations and considerations taken for each component in the boost stage are detailed in sections 4.1, 4.2, 4.3, 4.4 and 4.5.

The proposed design needs to accommodate the possibility of implementing a tracking algorithm within the control loop. This and other peripheral connections are detailed in the following sections.

6.1 Boost Stage

The proposed boost stage follows the schematic depicted in figure 6.1.

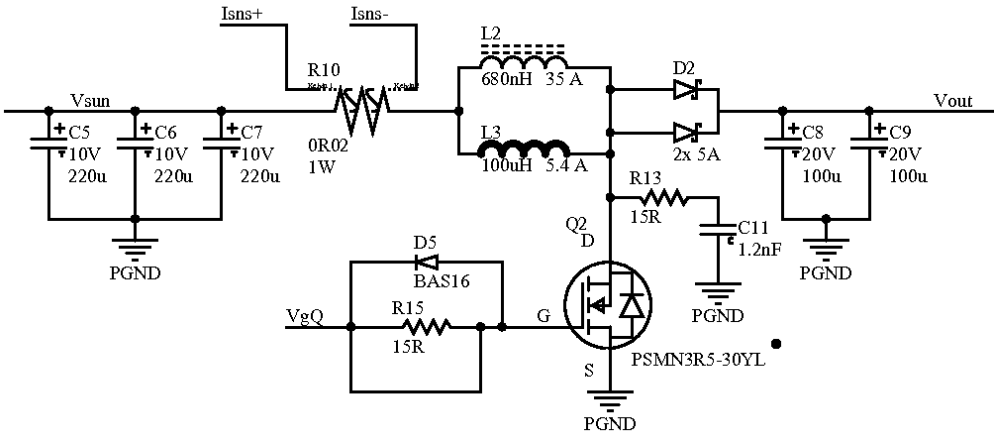


Figure 6.1: Schematic of Boost Stage

From figure 6.1 we can identify the core components which have been calculated in chapter 4. Not mentioned yet present are the current sense resistor and the optional gate drive turn on/off circuit.

6.1.1 Sense resistor

If this circuit were to be used in a final application, the sense resistor would not be extracted from the design as it only introduces a power loss. The proposed design is to evaluate the feasibility of such a converter

and therefore the sense resistor has been added as an observation variable. To improve the precision of the current measurement the footprint of the SMD resistor incorporates Kelvin contacts. The circuit attached to the Kelvin contacts of the sense resistor is a current sense chip from Linear Technologies, the LT1787. This chip and a couple of operational amplifiers are sourced externally with a dual rail supply to reduce the influence on the energy conversion process. The operational amplifiers adapt the readings to an output which is meant to be visualized on an oscilloscope.

6.1.2 Gate drive circuit

turn on/off circuit

This is a typical circuit used in many mosfet drives. The paralleled resistor and diode provide asymmetric paths for the sourcing and sinking currents. The mosfet is a voltage governed device but it has a gate to source capacitance which needs to be charged/discharged to reach the threshold levels activating/deactivating the device.

In the turn on phase, sourcing current, the current flows through the resistor and the speed at which the gate is charged is dependent on the resistance and defined as

$$\tau = R \cdot C_{gs} \tag{6.1}$$

In the turn off phase, sinking current, the current flow is aided by the diode which is now forwardly biased and therefore the turn off time is shorter than the turn on time.

Drive Circuit

The current limited by turn on/off circuit, $\approx$ 70mA, exceeds the maximum output current specifications, 20mA, of the micro controller which will be used. Normally one would simply use an integrated output drive circuit such as the ISL5510, IC2 in figure 6.2, but the minimum voltage specifications are above our startup voltage requirements. This has led me to implement a discrete push-pull stage, shown in figure 6.2.

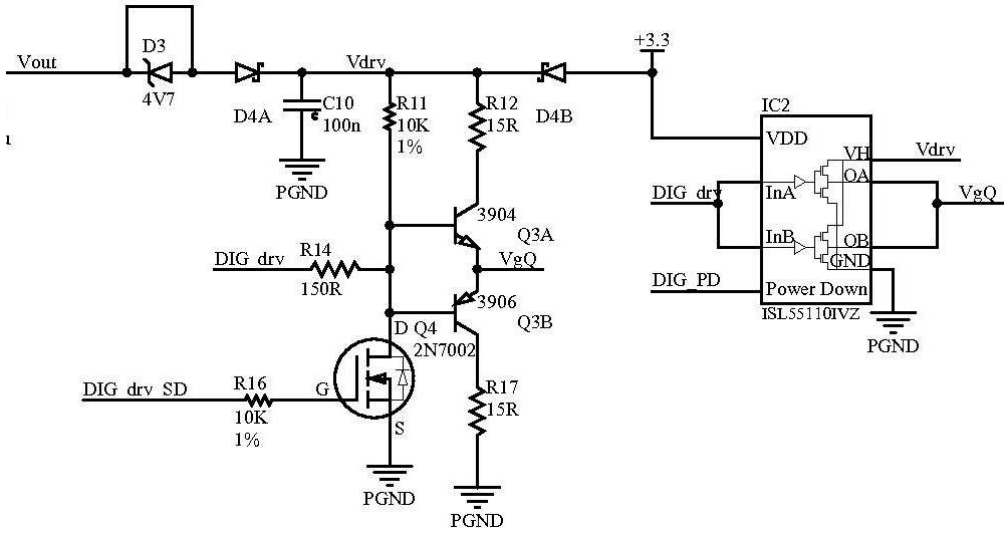


Figure 6.2: Schematic of Mosfet Gate Drive

The mosfet Q_4 has been added to be able to shutdown the gate drive if needed. The initial driving voltage is given by a pre-stepup circuit, described in section 6.2, which should allow for a low loading start up. The diodes, D_4A and D_4B allow the drive voltage to grow as our main converter begins to output voltage. D_3 can decrease the drive voltage by the zener drop.

6.2 Pre-Step up

The main converter is required to extract power from the solar cells with a Maximum Power Point Tracking algorithm down to a minimum voltage level which is below the minimum operating voltage of the micro controller destined to implement this tracking.

The main power control loop in implemented with a micro controller as the heart and requires a voltage of at least 2 volts DC to start pumping. The MPPT algorithm is required to work down to a voltage level of 700mV. To activate the electronics, initially this voltage will be brought up by means of a low power step-up converter, the pre-step up. Once the main converter is in the system will obtain the required energy from the main converter leaving the pre-step up in operative. Figure 6.3 shows the pre-step up.

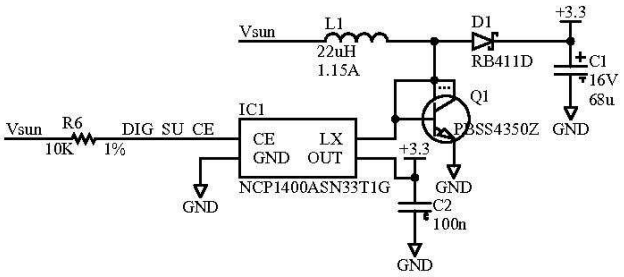


Figure 6.3: Pre Step up Schematic

6.3 Micro controller

The micro controller suggested for this application is the Microchip PIC 16F690. This chip offers a wide operating voltage of 2.0-5.5 volts, up to 12 channels of 10-bit Analog to Digital converter, an analog comparator module with two comparators, programmable on-chip voltage reference, and an Enhanced Capture/Compare/PWM with dead band delay. The interconnections on the designed board are shown in figure 6.4.

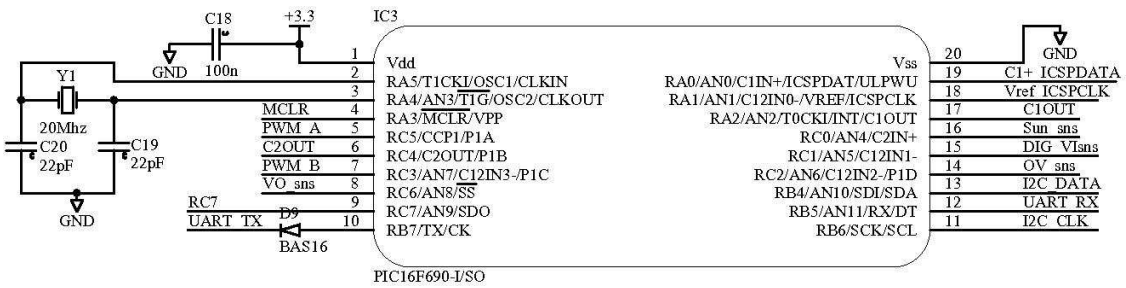


Figure 6.4: Micro controller peripheral connections

The interconnections have been made to be able to implement several of the algorithms described in chapter 5.

6.3.1 Inputs

The analog inputs can be converted referenced to the supply rail voltage or to an external source. Since our supply voltage is the output of boost converter there will be some ripple. This will result in a resolution loss in our measurements. Besides the ripple we are also subject to output voltage fluctuations much larger than those of the expected ripple. To solve this an external reference voltage with a JFET, as shown in figure 6.5, is used as the analog reference voltage for the analog to digital conversion.

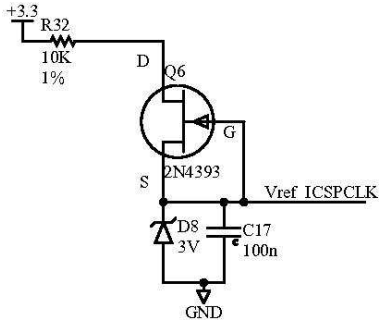


Figure 6.5: Analog reference voltage

Sensing

All sensing inputs are derived from a voltage divider to ensure that the maximum input voltages are not exceeded.

- Sun_sns: This senses the solar cell output voltage.
- Dig_VIsns: This is connected to the output of the current sense circuit described in section 6.1.1.
- OV_sns&VO_sns: Two output voltage sense nodes with seperate voltage divider circuits.
  - OV_sns is proposed to be added to connected to a comparator input where and over voltage condition may trigger a change in behaviour

6.3.2 Outputs

- C1OUT: Used to optionally drive the mosfet using the sensed current as a duty defining parameter
- C2OUT: Output connected to shutdown the drive circuit in case of an over voltage event
- PWM_A&PWM_B: PWM outputs which can either directly drive the mosfet or used as a digital to analog converter when passed through a low pass filter.
- RC7: A free pin which has been routed to the shutdown pins of different circuits.

6.3.3 External interface

The PICkit2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging. The design makes the pins available for the ICSP programming and In-Circuit-Debug interface where, besides programming the board, there are additional tools which allow us to capture the digital waveforms of several pins in our circuit, thereby substituting the need for a logic analyzer.

Communication

In the event that this board would like to be integrated into a larger system, a couple common serial channels have been made available.

For a point-to-point communication the wide spread USART is made available to be able to provide a simple and basic communication to the micro controller. This intended use is for debugging purposes as this is not a very robust communication channel.

For a multi-node communication, I^2C[1] pins have been also made available. I^2C uses only two bidirectional open-drain lines, Serial Data Line(SDA) and Serial Clock (SCL), pulled up with resistors. It is appropriate for peripherals where simplicity and low manufacturing cost are more important than speed. For added robustness the SMBus[2] protocol can be implemented.

[1] I^2C: Inter-Integrated Circuit, multi-master serial single-ended computer bus invented by Phillips
[2] SMBus is a subset of I^2C that defines stricter electrical and protocol conventions.

6.4 Economical analysis

The development of this project can be broken down into the following stages:

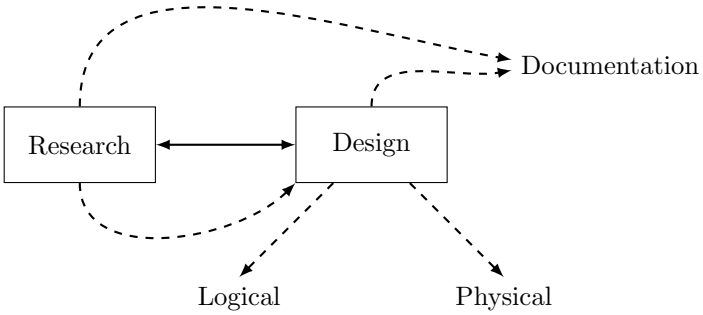


Figure 6.6: Main stages in project design

As can be seen from figure 6.6, all main sections are tied together and there is constant feedback from one section to another. No doubt, when given a project idea the main occupation is research until the concept involving what has to be done is understood. Then creativity has to come in to find a solution to the problem posed, which again requires research but the design phase has started. Given the vast amount of literature on the subject the research can be considered inefficient towards the true objective, although the acquired knowledge can come in handy with future projects.

The logical part of the design phase consists of functional design with basic circuit ideas and circuit simulations, although the latter could be included in research. The physical part is when the something real has to be developed and the "ideal" behavior of the functional parts developed needs to be brought to existing components. This is when real component values are calculated, schematics get completed and the printed circuit board routed.

Documentation, by far the most important and least looked after part of projects in general. Although not as much time as should have was put into this part it is the most worth full part of the project. A board design without a detailed explanation of its internal working can not be developed successfully.

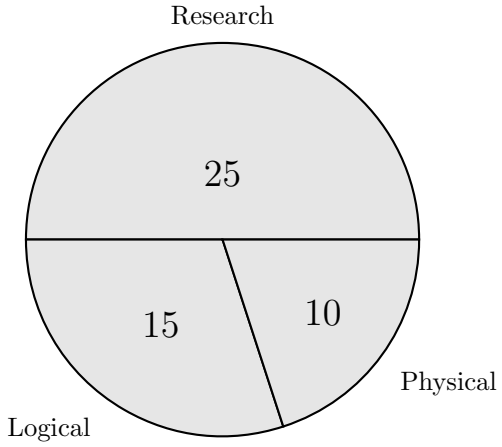


Figure 6.7: Time consumption on different processes [units in days]

Conclusion & Future Lines

Conclusion

A design has been proposed to evaluate the feasibility of the classical boost converter in the posed scenario. Rather than a solution to the problem posed, the design has served the purpose of understanding the problems and limitations that appear in high voltage gain scenarios.

From the explained topologies the tapped boost converter appears to be the most adequate for high voltage gain applications, yet the current limitations in actual coupled inductors for small sized environments limits the power output capabilities. The multi phase boost topology in conjunction with the tapped inductor topology is the most promising solution with the given research.

The variations of theoretical design to the actual practical design have been noted when the components for an actual boost converter were calculated. These variations are still based on mathematical relationships gathered from experimental results reviewed in multiple papers and would require an experimental validation to guarantee the design objective and liability.

Of the vast amount available, the maximum power point tracking algorithms presented all have trade offs of simplicity versus accuracy. Given the hardware of the proposed design, the Hill Climbing / Perturbation and observation algorithm appears to be the most fitting.

The research done has the purpose of expanding the choices of topologies and algorithms to applications of power scavenging. A topic who's' general interest is growing for remote and portable electronics. The thesis should serve as a reference for developing projects of similar objectives.

Future Lines

Translate MPPT Algorithms

From the mathematical equations and described functionality to pseudo code, high-level language and possibly machine level language, to be able to incorporate the code in other projects.

Implementation and evaluation

Having proposed a design for evaluating the application of a classical boost converter in a high gain scenario, the first step to further understanding the assumed concepts will be to implement the design and evaluate the limitations. Not only the analog limitations but also the flexibility and convergence rate of the MPPT algorithms implemented.

Evolution of the design

Having introduced the multiphase boost and tapped boost topologies, the design could be extended to incorporate these topologies. A combination of both may result in the most efficient design. At a micro controller integration level, the PIC16F product family is classified as a level 2 integration, Proportional Control. Further levels include Topology Control, which provide added hardware such as an integrated multiplier and a faster analog to digital converter. Going to the top level classified as Digital Control, where micro controllers with high performance DSP engines along with other specialized peripherals are available to implement the control algorithms. Evaluating the need to evolve to a more complex micro controller and the added energy cost.

Analyze other boost topologies

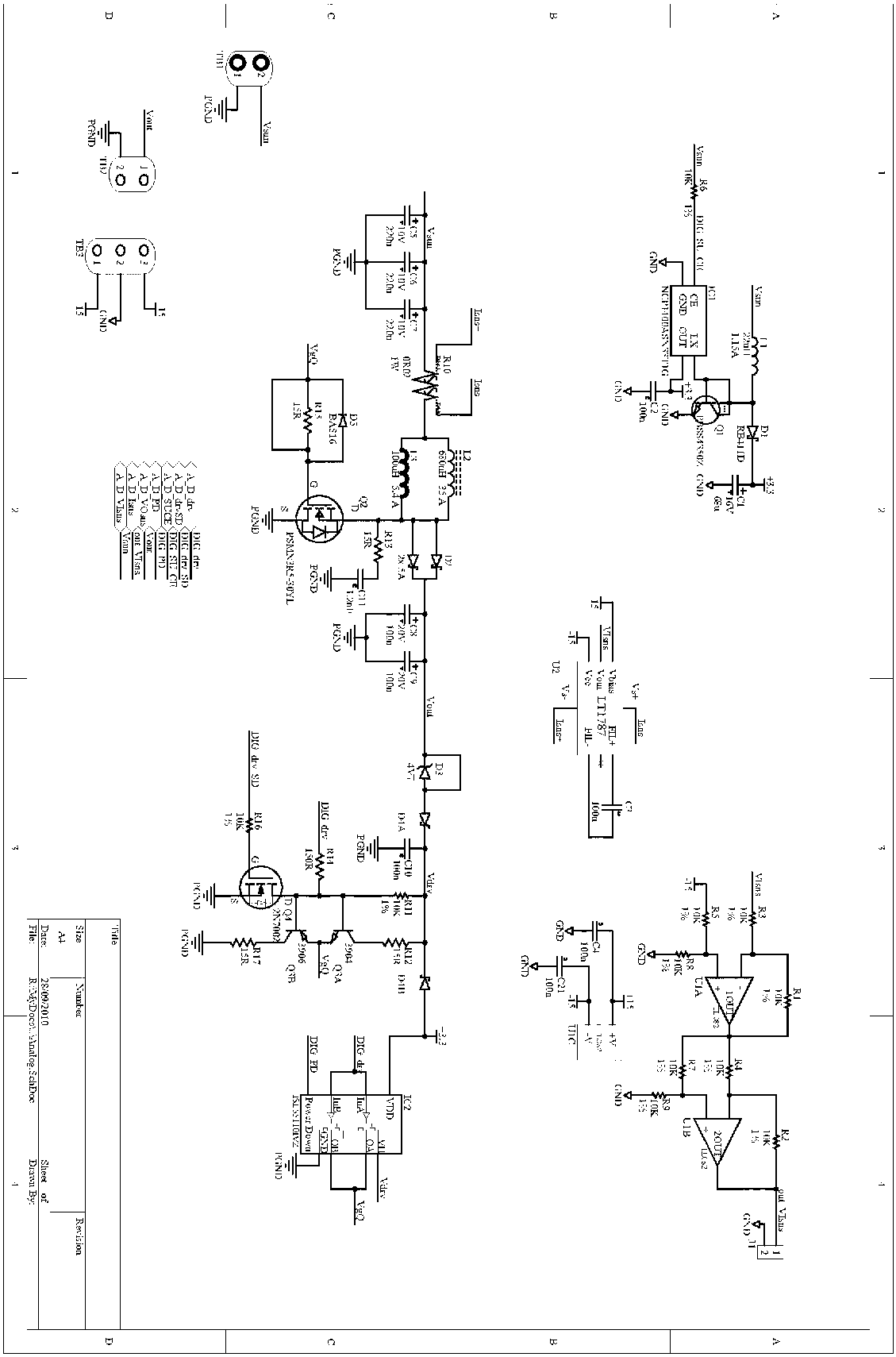
Their are a vast amount of boosting topologies, with in which some very interesting one based on resonant voltage elevation. While in the phase of research I stumbled across some papers by *Fang Lin Luo* and *Hong Ye* which propose scalable circuit configurations with duty gain relationships such as:

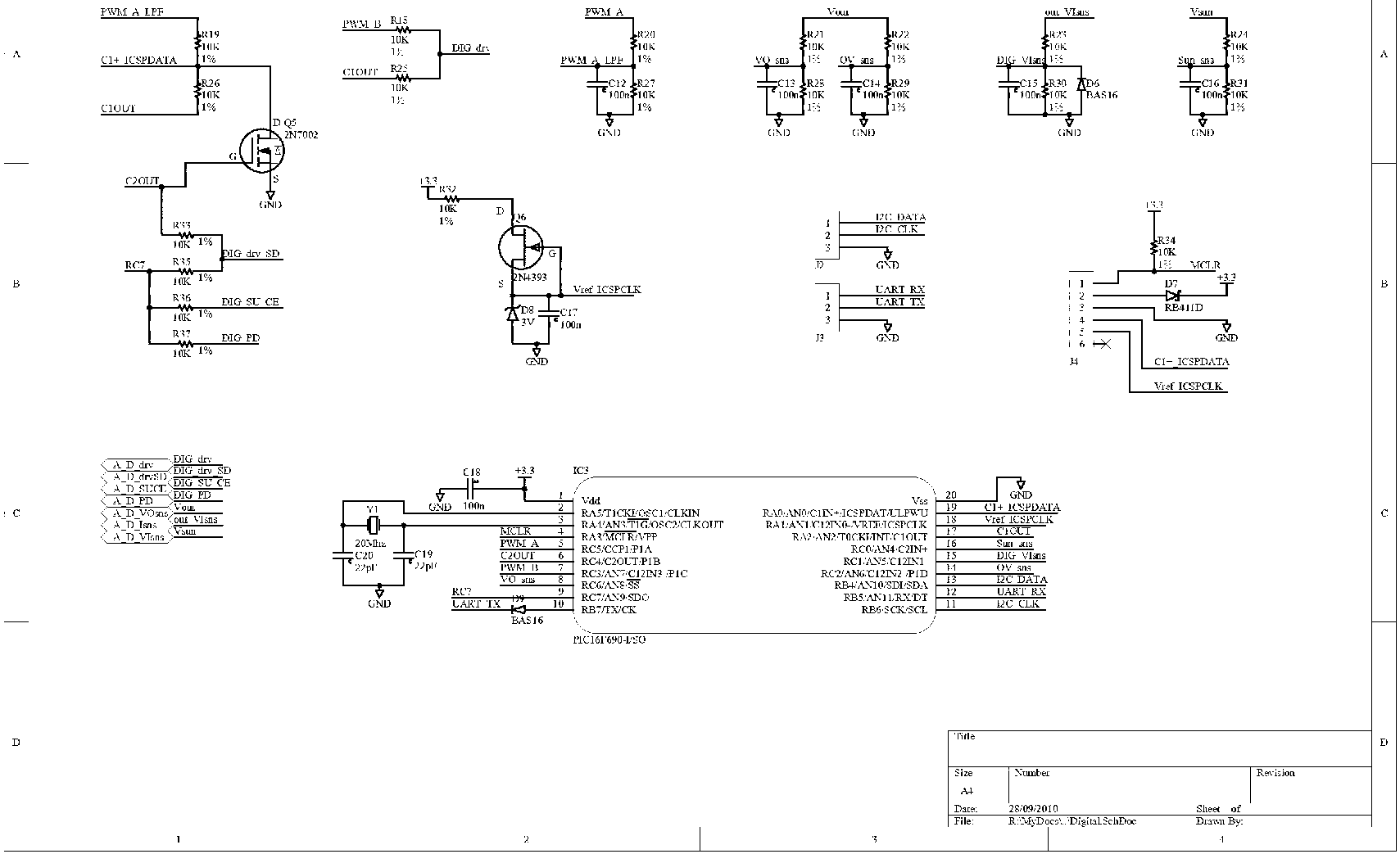
$$\frac{V_{out}}{V_{in}} = \left(\frac{4-k}{1-k}\right)^n$$

where n is the number of stages. These call themselves Luo converters.

Appendix A

Schematics




PWM A LPF
R19 10K 1%
C1+ ICSPDATA
R26 10K 1%
C1OUT
D Q5 2N7002
G
S
GND
C2OUT
R33 10K 1%
DIG drv SD
RC7
R35 10K 1%
R36 10K 1%
DIG SU CE
R37 10K 1%
DIG PD
PWM B
R15 10K 1%
DIG drv
C1OUT
R25 10K 1%
PWM A
R20 10K 1%
PWM A LPF
C12 100n
R27 10K 1%
Vout
R21 10K 1%
VO sns
C13 100n
R28 10K 1%
OV sns
C14 100n
R29 10K 1%
out VIsns
R23 10K 1%
DIG VIsns
C15 100n
R30 10K 1%
D6 BAS16
Vsun
R24 10K 1%
Sun sns
C16 100n
R31 10K 1%
3.3
R32 10K 1%
D
Q6
G
2N4393
S
Vref ICSPCLK
D8 3V
C17 100n
I2C DATA
I2C CLK
J2
UART RX
UART TX
R24 10K 1%
MCLR
+3.3
D7 RB411D
J4
C1- ICSPDATA
Vref ICSPCLK
A_D drv
A_D drvSD
A_D SUCE
A_D PD
A_D VOsns
A_D Isns
A_D VIsns
DIG drv
DIG drv SD
DIG SU CE
DIG PD
Vout
out VIsns
Vsun
C18 100n
+3.3
Y1 20Mhz
C20 22pF
C19 22pF
IC3
Vdd
RA5/T1CKI/OSC1/CLKIN
RA4/AN3/T1G/OSC2/CLKOUT
RA3/MCLR/VPP
RC5/CCP1/P1A
RC4/C2OUT/P1B
RC3/AN7/C12IN3 /P1C
RC6/AN8/SS
RC7/AN9/SDO
RB7/TX/CK
MCLR
PWM A
C2OUT
PWM B
VO sns
RC7
UART TX
D9 BAS16
Vss
RA0/AN0/C1IN+/ICSPDAT/ULPWU
RA1/AN1/C12IN0-/VREF/ICSPCLK
RA2/AN2/T0CKI/INT/C1OUT
RC0/AN4/C2IN+
RC1/AN5/C12IN1
RC2/AN6/C12IN2 /P1D
RB4/AN10/SDI/SDA
RB5/AN11/RX/DT
RB6/SCK/SCL
GND
C1+ ICSPDATA
Vref ICSPCLK
C1OUT
Sun sns
DIG VIsns
OV sns
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UART RX
I2C CLK
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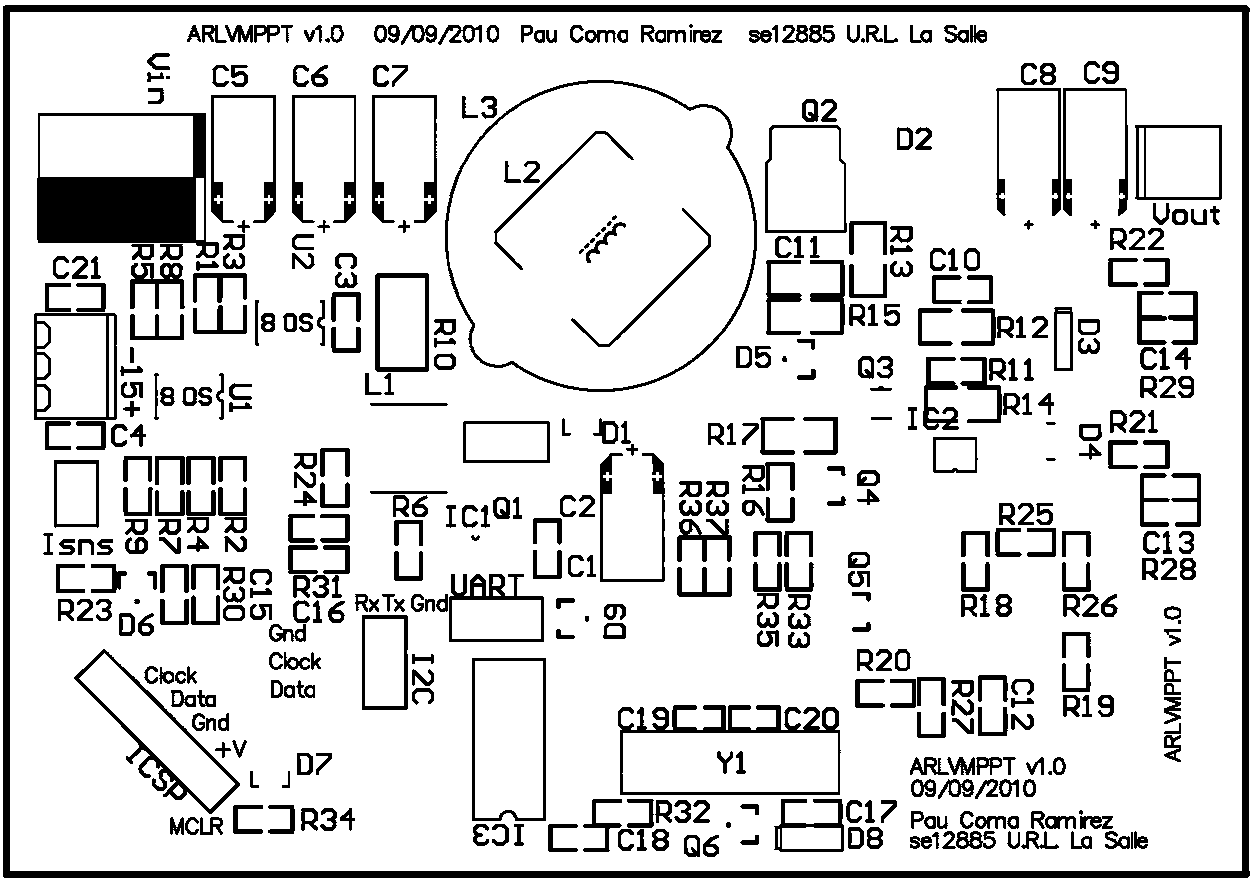
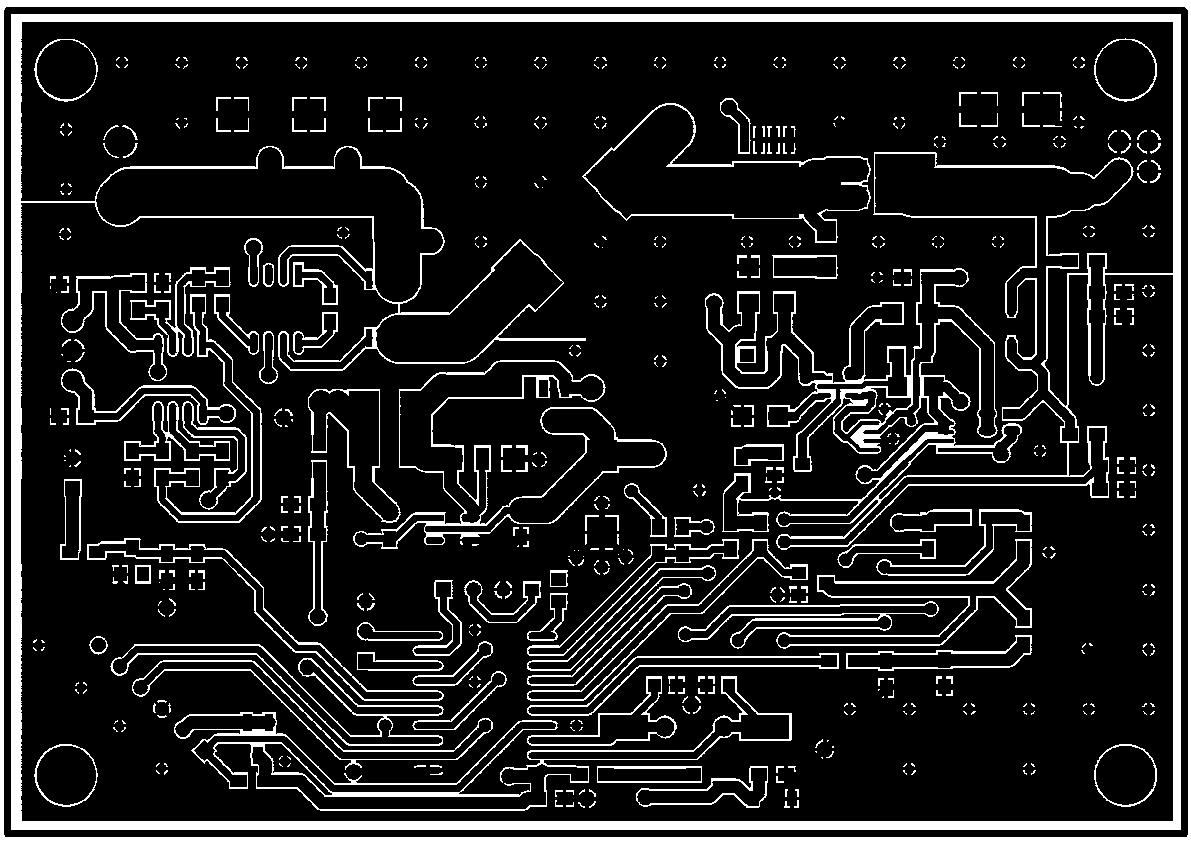
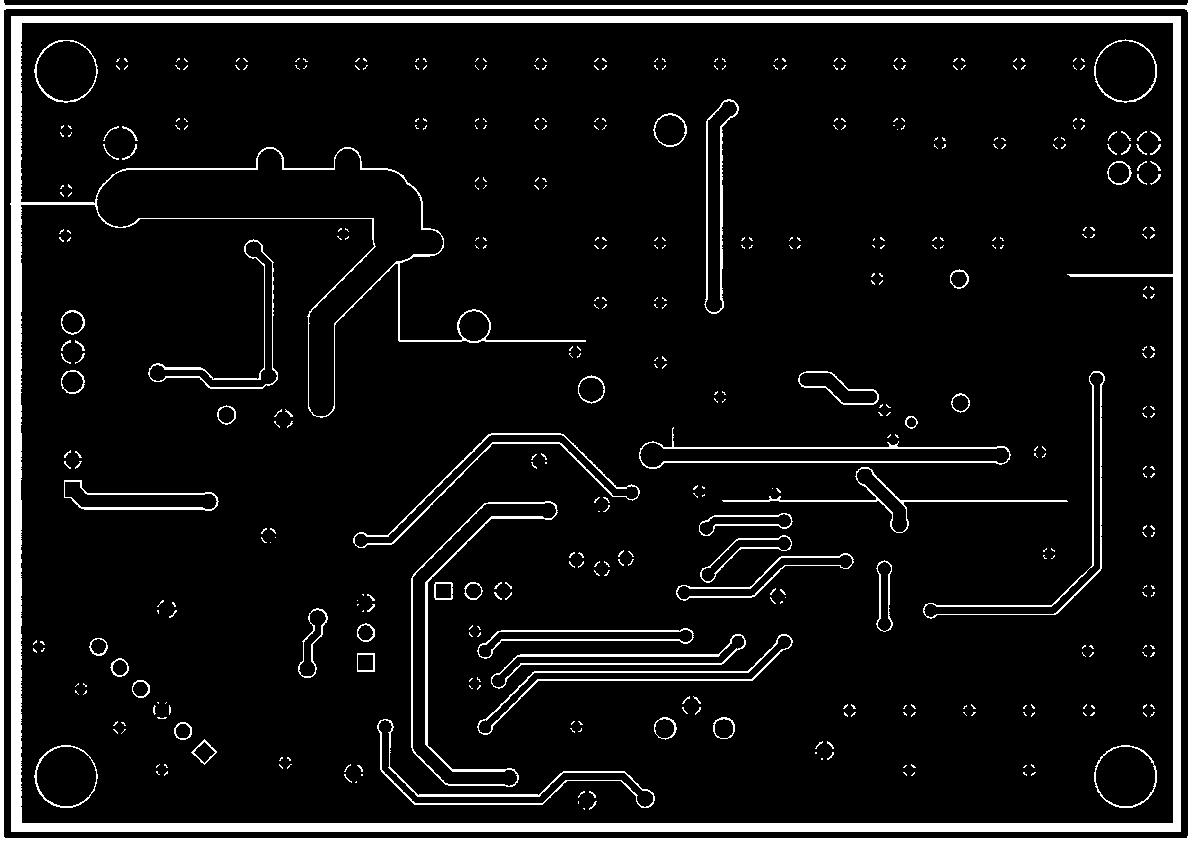
Appendix B

Printed Circuit Board







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